Device Modeling Report

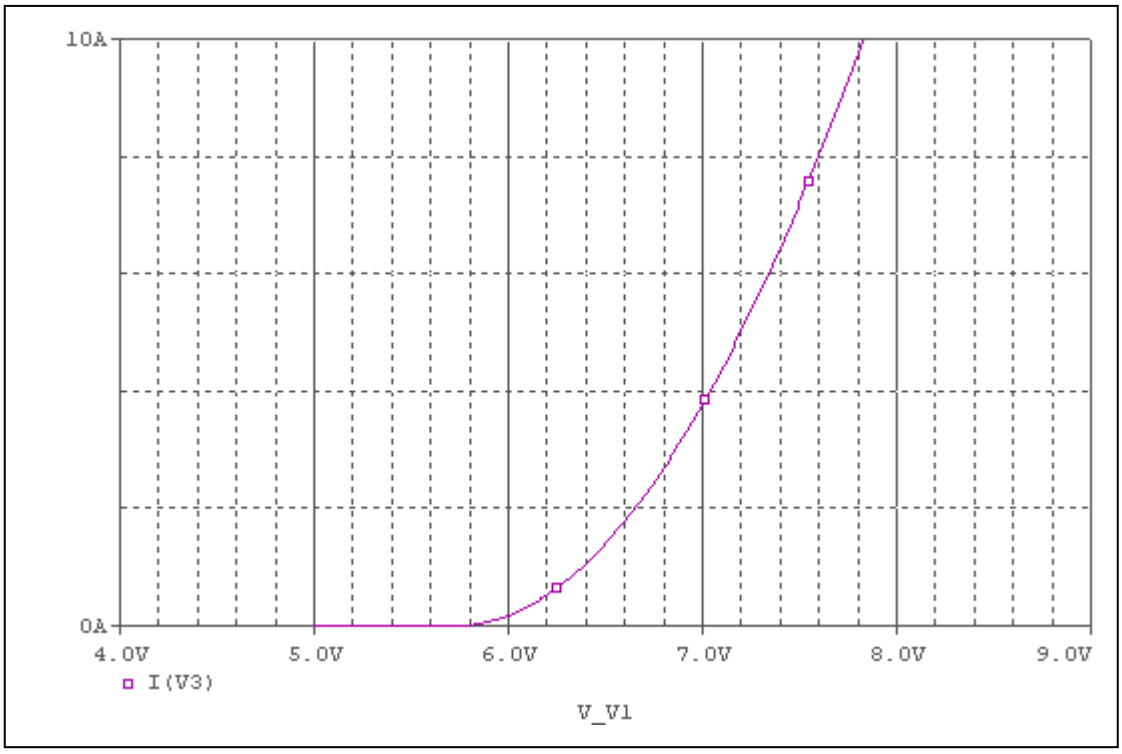
COMPONENTS: Insulated Gate Bipolar Transistor (IGBT)
PART NUMBER: IRG4BC20SD-S
MANUFACTURER: International Rectifier

Bee Technologies Inc.

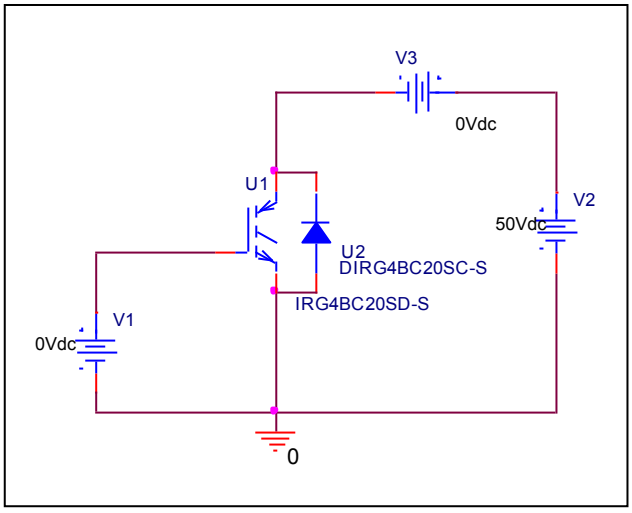
Pspice model parameter	Model description
TAU	Ambipolar Recombination Lifetime
KP	MOS Transconductance
AREA	Area of the Device
AGD	Gate-Drain Overlap Area
WB	Metallurgical Base Width
VT	Threshold Voltage
KF	Triode Region Factor
CGS	Gate-Source Capacitance per Unit Area
COXD	Gate-Drain Oxide Capacitance per Unit Area
VTD	Gate-Drain Overlap Depletion Threshold

Transfer Characteristics

Circuit Simulation result

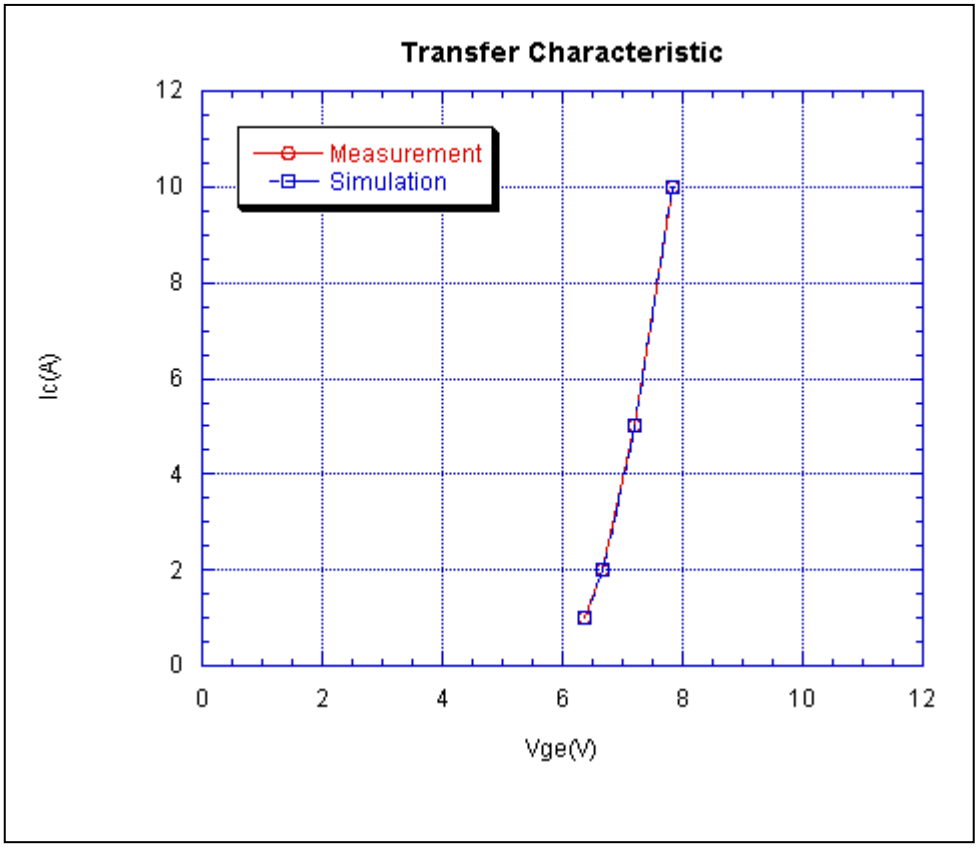


Evaluation circuit



Comparison Graph

Circuit Simulation Result



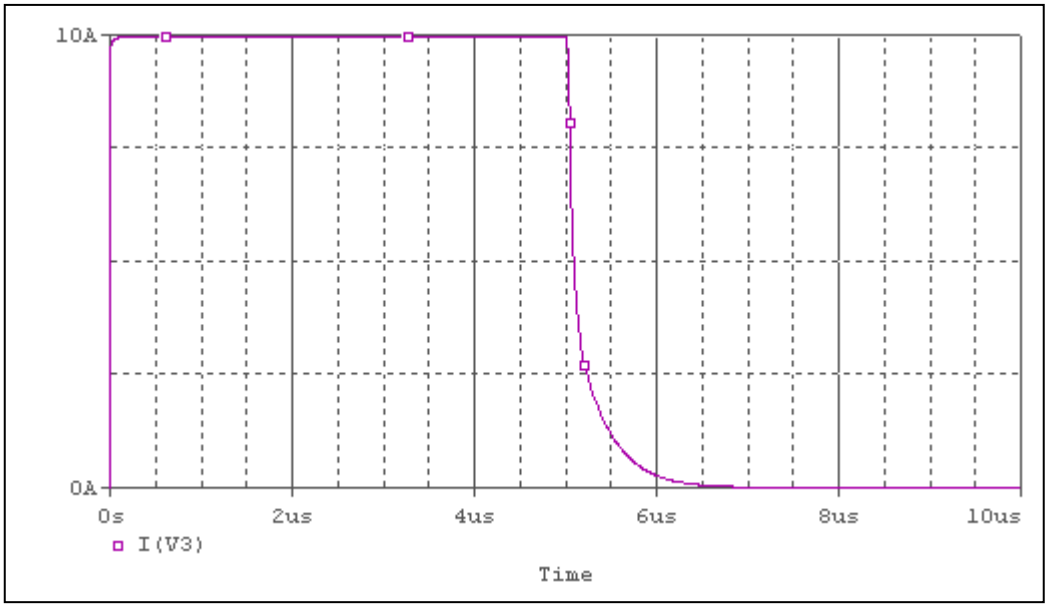
Simulation Result

Test condition : Vce = 10 V

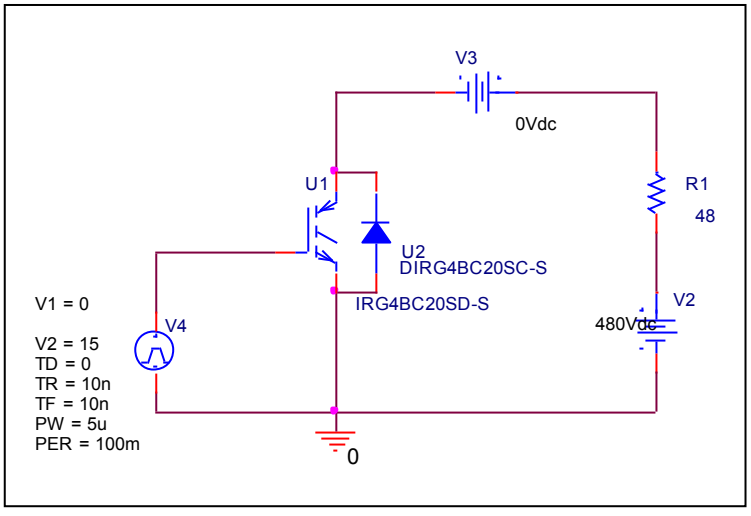
Ic(A)	Vge(V)		Error (%)
	Measurement	Simulation	
1	6.38	6.3799	-0.00157
2	6.66	6.6524	-0.11411
5	7.19	7.1991	0.12656
10	7.83	7.8258	-0.05364

Fall Time Characteristics

Circuit Simulation result



Evaluation circuit

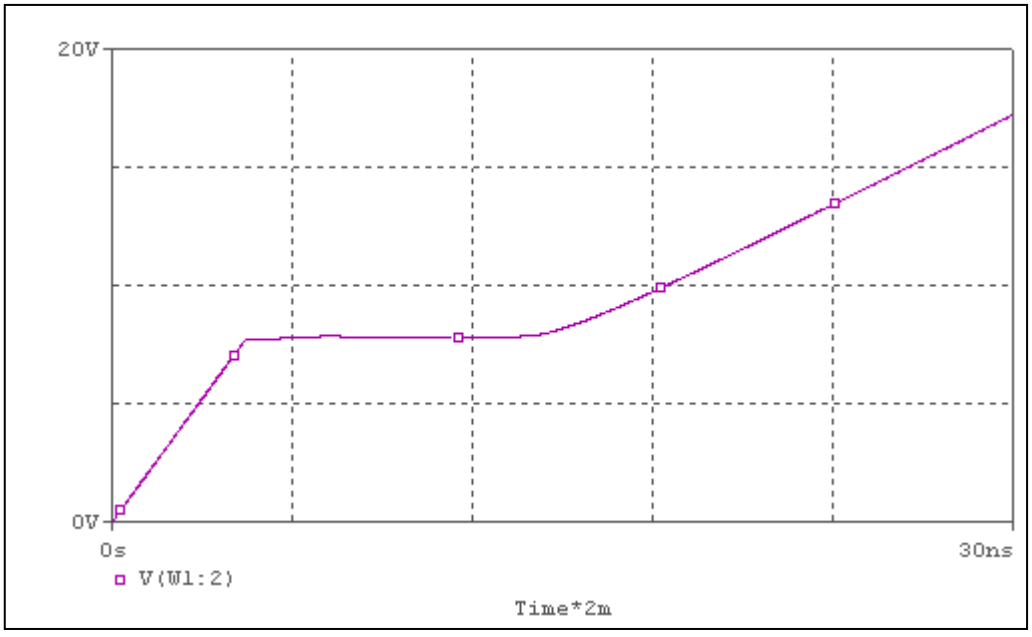


Test condition Ic=10(A) ,Vcc=480(V)

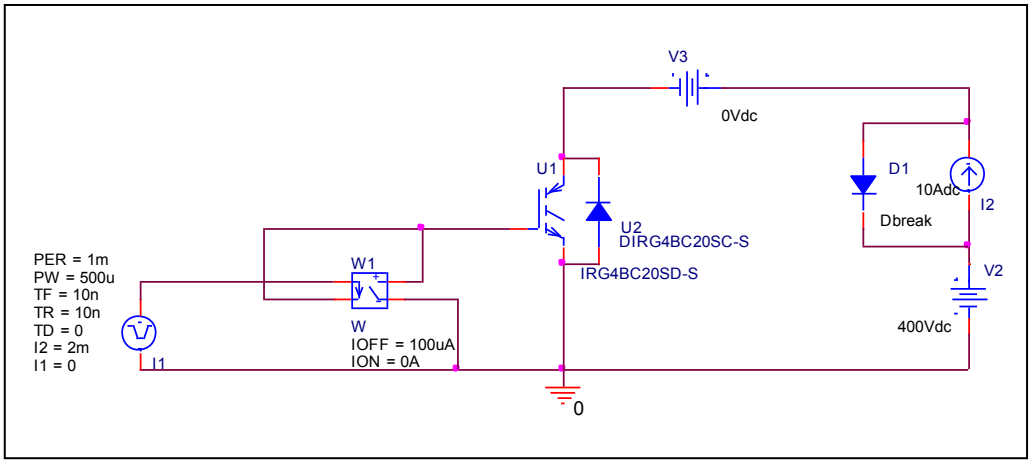
tf	Measurement		Simulation	
	480[Typ.]~730[Max.]	ns	518.392	ns

Gate Charge Characteristics

Circuit Simulation result



Evaluation circuit

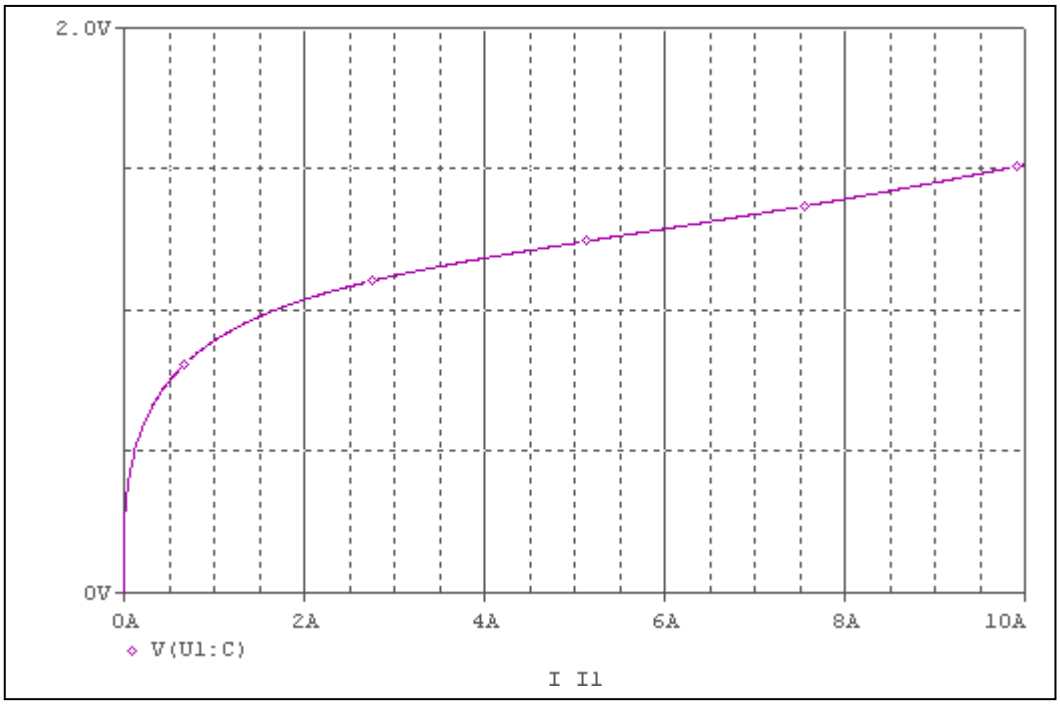


Test condition : Vcc=400(V) ,Ic=10(A) ,Vge=14(V)

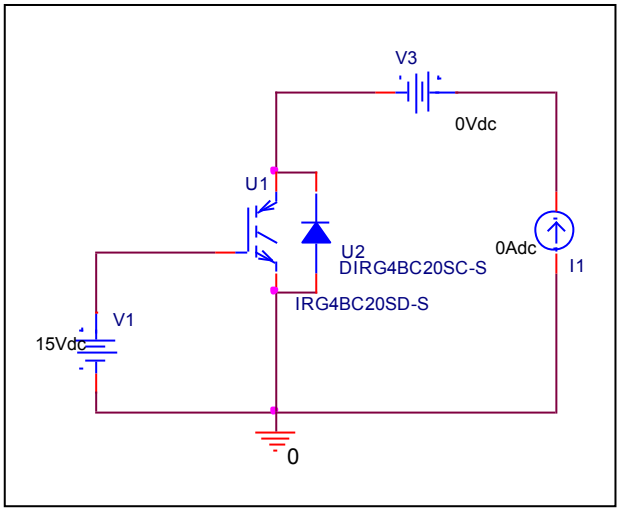
	Measurement		Simulation		Error(%)
Qge	4.5	nc	4.4690	nc	-0.6888
Qgc	10	nc	9.956	nc	-0.4400
Qg	25	nc	25	nc	0.0

Saturation Characteristics

Circuit Simulation result

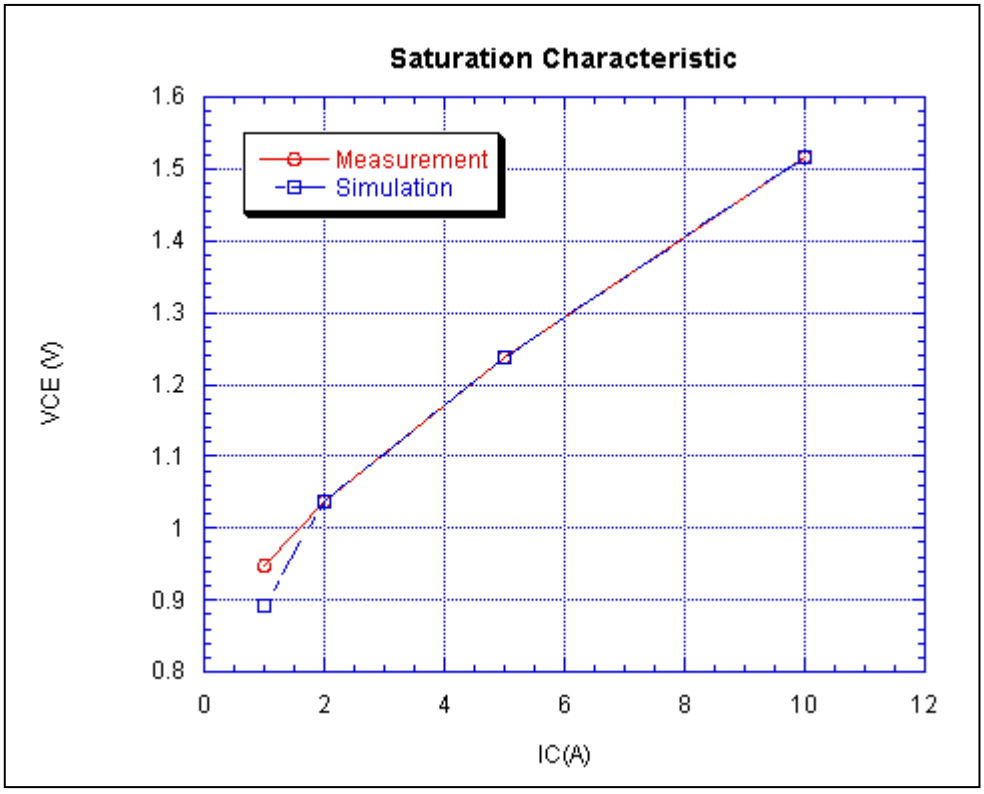


Evaluation circuit



Comparison Graph

Circuit Simulation Result

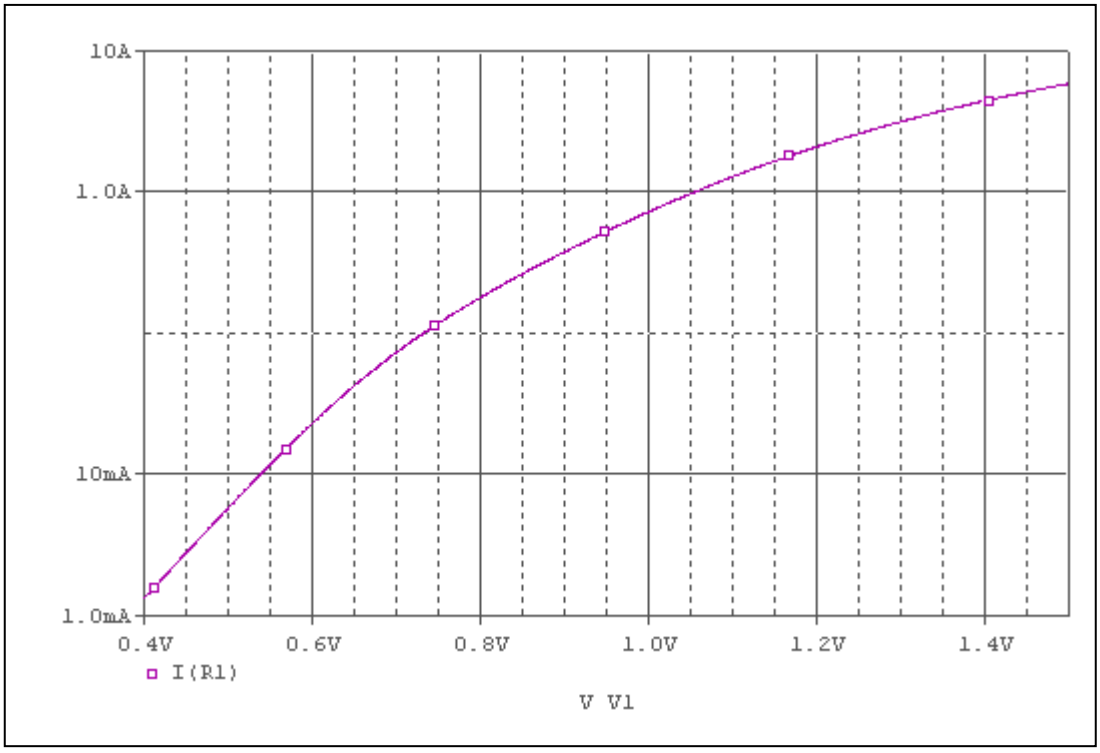


Simulation Result

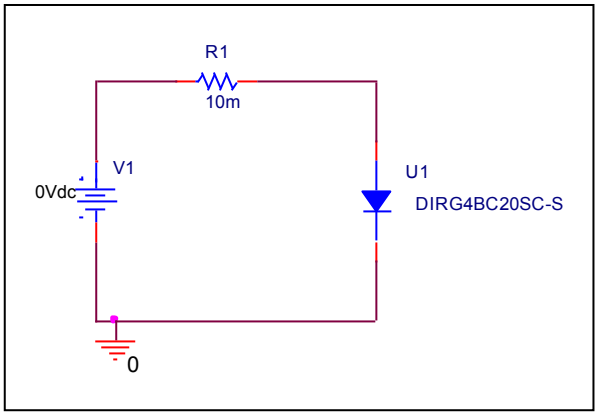
Ic(A)	Vce(sat)(V)		Error (%)
	Measurement	Simulation	
1	0.948	0.892345	-5.87078
2	1.038	1.038	0.00000
5	1.238	1.238	0.00000
10	1.516	1.5173	0.08575

Forward Current Characteristic

Circuit Simulation Result

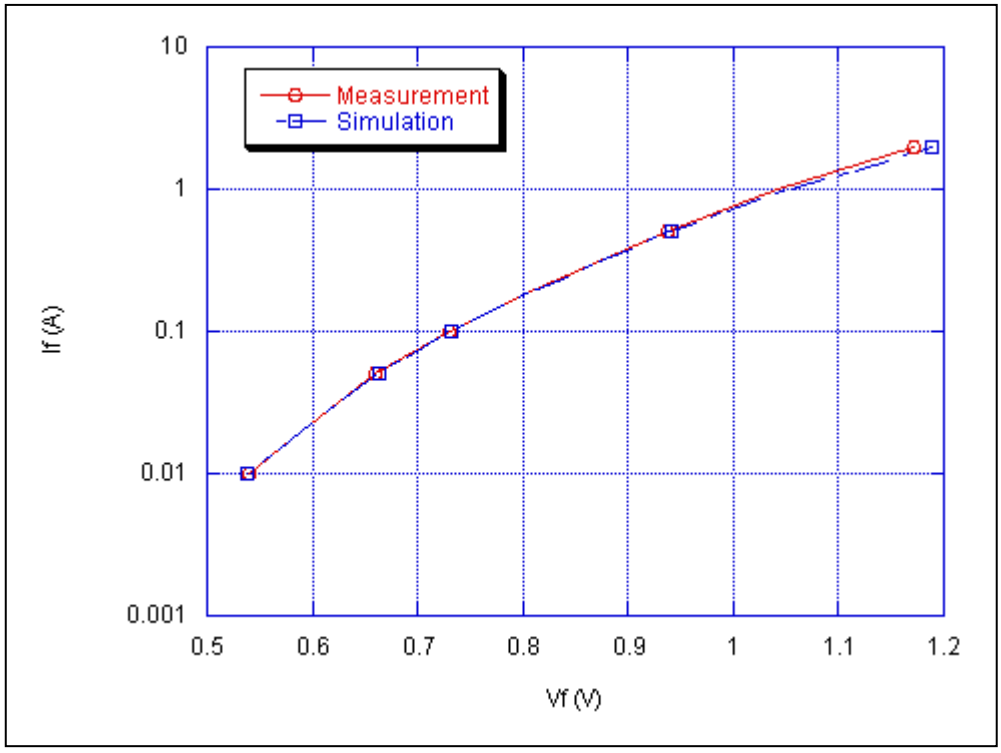


Evaluation circuit



Circuit Simulation Result

Comparison graph

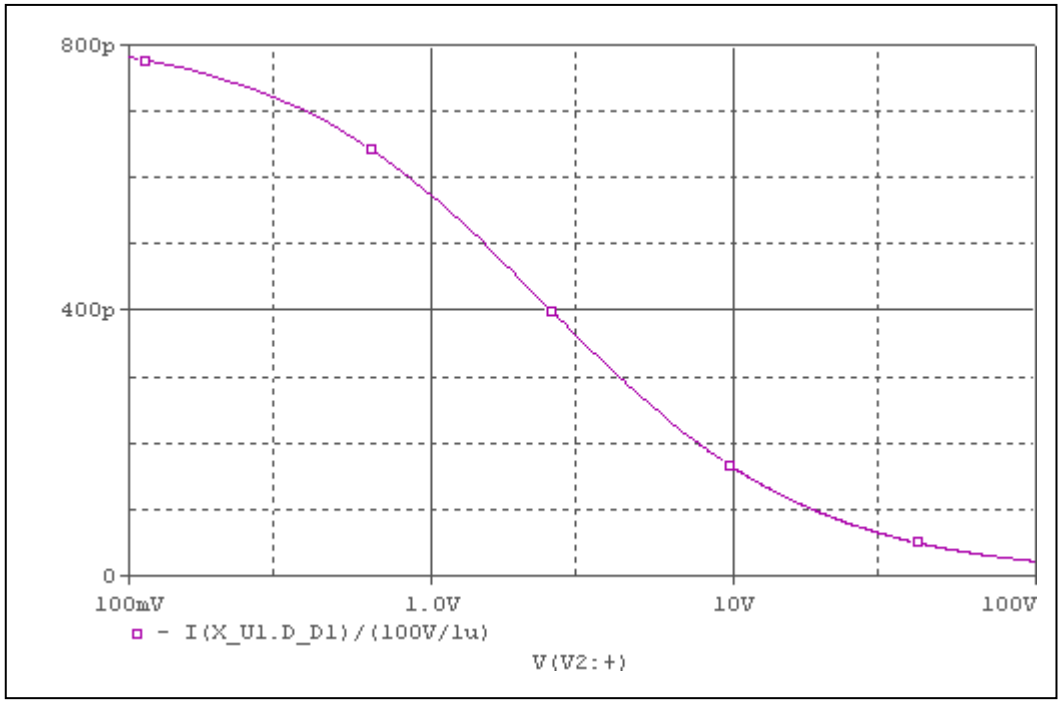


Simulation Result

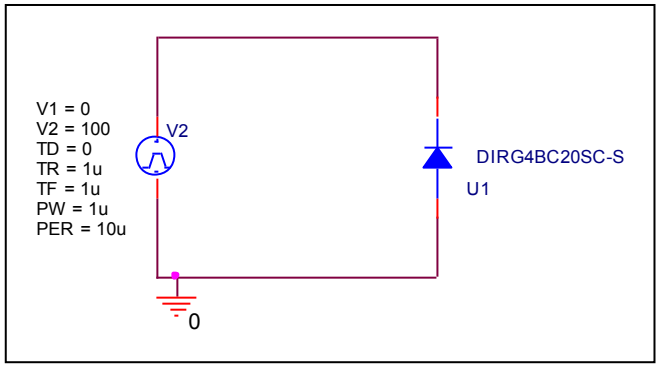
Ifwd (A)	Vfwd(V) Measurement	Vfwd(V) Simulation	%Error
0.01	0.54	0.538125	-0.34722
0.02	0.59	0.589480	-0.08814
0.05	0.66	0.664104	0.62182
0.1	0.73	0.732538	0.34767
0.2	0.812	0.814142	0.26379
0.5	0.938	0.942460	0.47548
1	1.042	1.0554	1.28599
2	1.172	1.1890	1.45051

Junction Capacitance Characteristic

Circuit Simulation Result

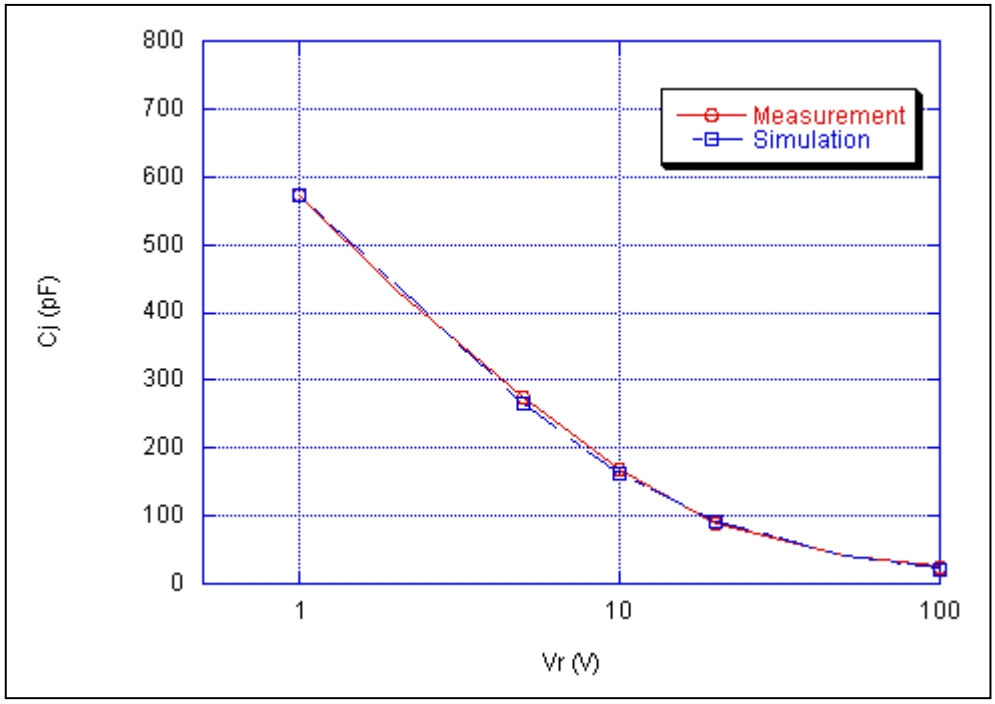


Evaluation circuit



Circuit Simulation Result

Comparison graph

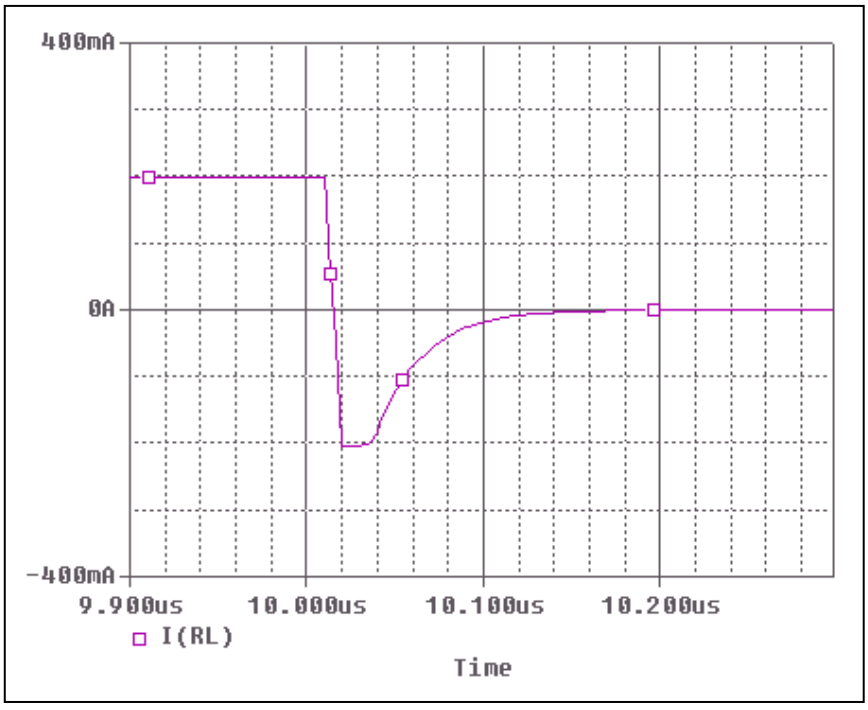


Simulation Result

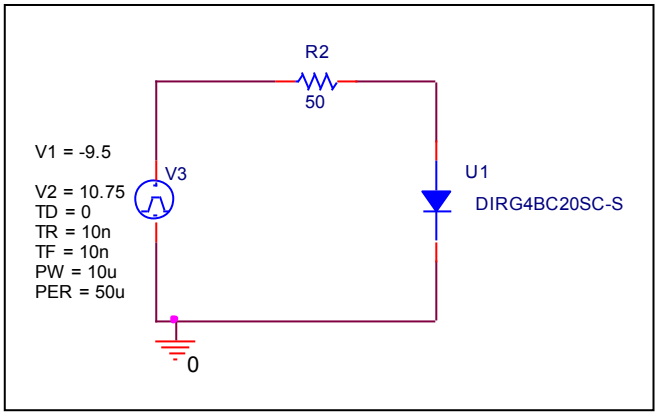
Vrev (V)	Cj(pF) Measurement	Cj(pF) Simulation	%Error
1	571.74	573.145	0.24574
2	433.5	443.203	2.23829
5	274.52	268.013	-2.37032
10	169.4	162.751	-3.92503
20	89	92.110	3.49438
50	42.98	41.081	-4.41833
100	22.9	21.770	-4.93450

Reverse Recovery Characteristic

Circuit Simulation Result



Evaluation circuit

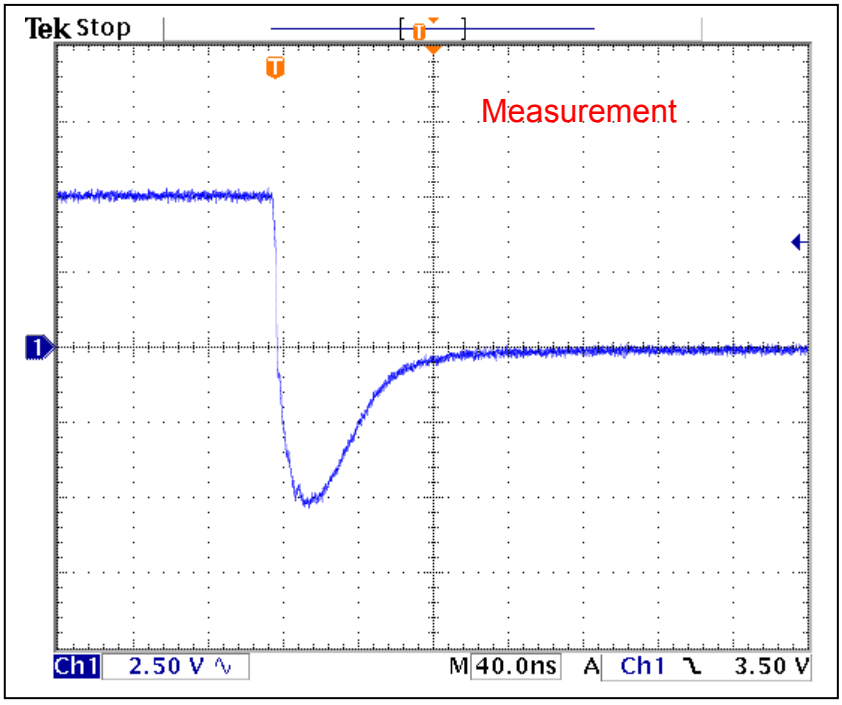


Compare Measurement vs. Simulation

	Measurement		Simulation		Error(%)
trj	20	ns	20.057	ns	0.28500
trb	62.4	ns	62.838	ns	0.70192

Reverse Recovery Characteristic

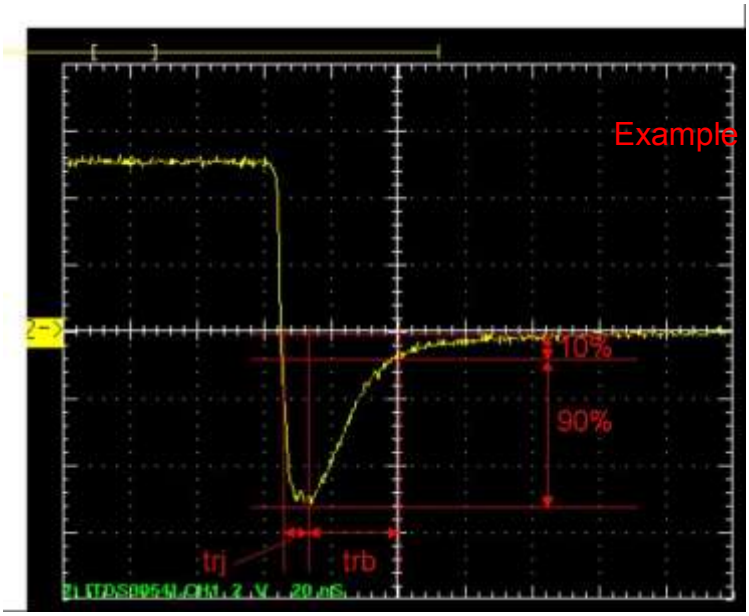
Reference



trj=20(ns)

trb=62.4(ns)

Conditions:Ifwd=Irev=0.2(A),Rl=50



Relation between trj and trb