Device Modeling Report

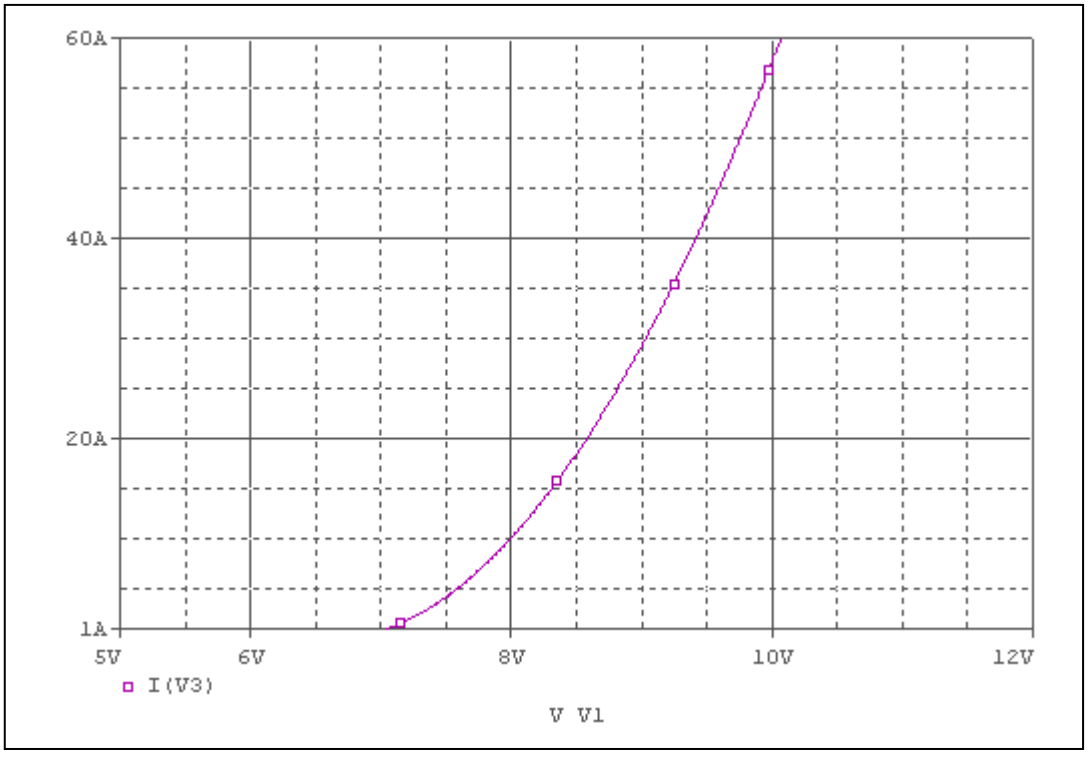
COMPONENTS: Insulated Gate Bipolar Transistor (IGBT)
PART NUMBER: IRG4PC50KD
MANUFACTURER: International Rectifier

Bee Technologies Inc.

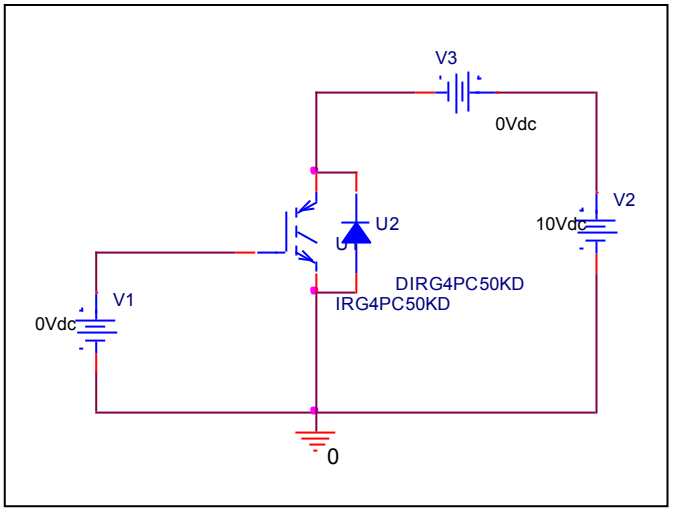
Pspice model parameter	Model description
TAU	Ambipolar Recombination Lifetime
KP	MOS Transconductance
AREA	Area of the Device
AGD	Gate-Drain Overlap Area
WB	Metallurgical Base Width
VT	Threshold Voltage
KF	Triode Region Factor
CGS	Gate-Source Capacitance per Unit Area
COXD	Gate-Drain Oxide Capacitance per Unit Area
VTD	Gate-Drain Overlap Depletion Threshold

Transfer Characteristics

Circuit Simulation result

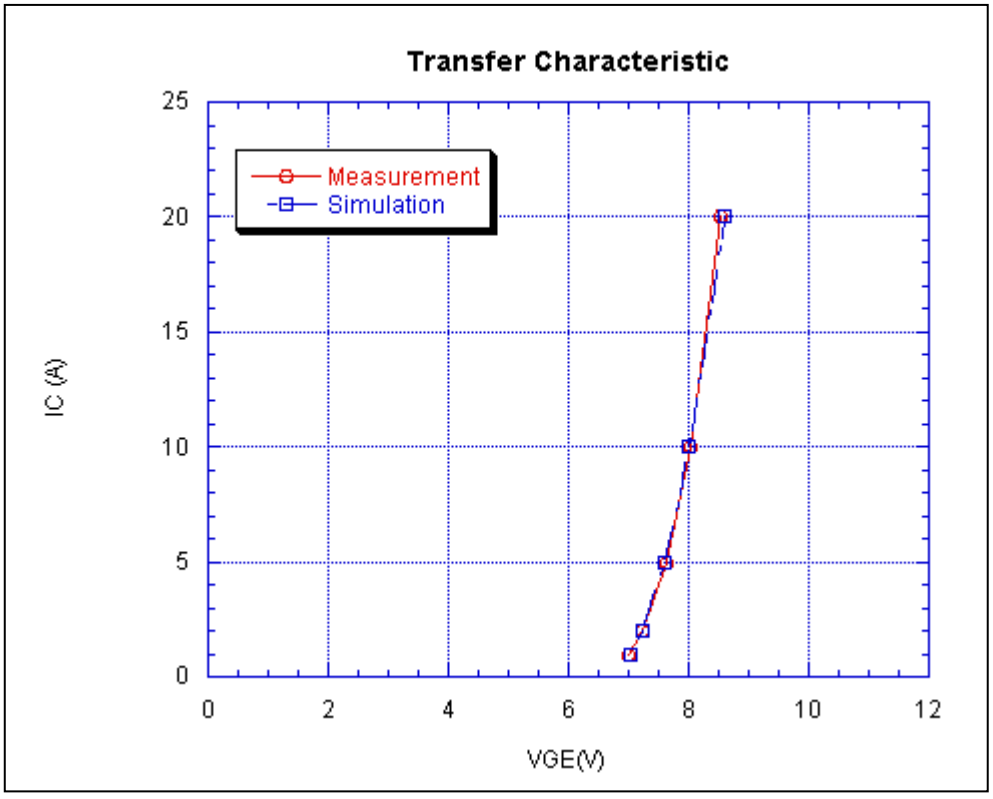


Evaluation circuit



Comparison Graph

Circuit Simulation Result



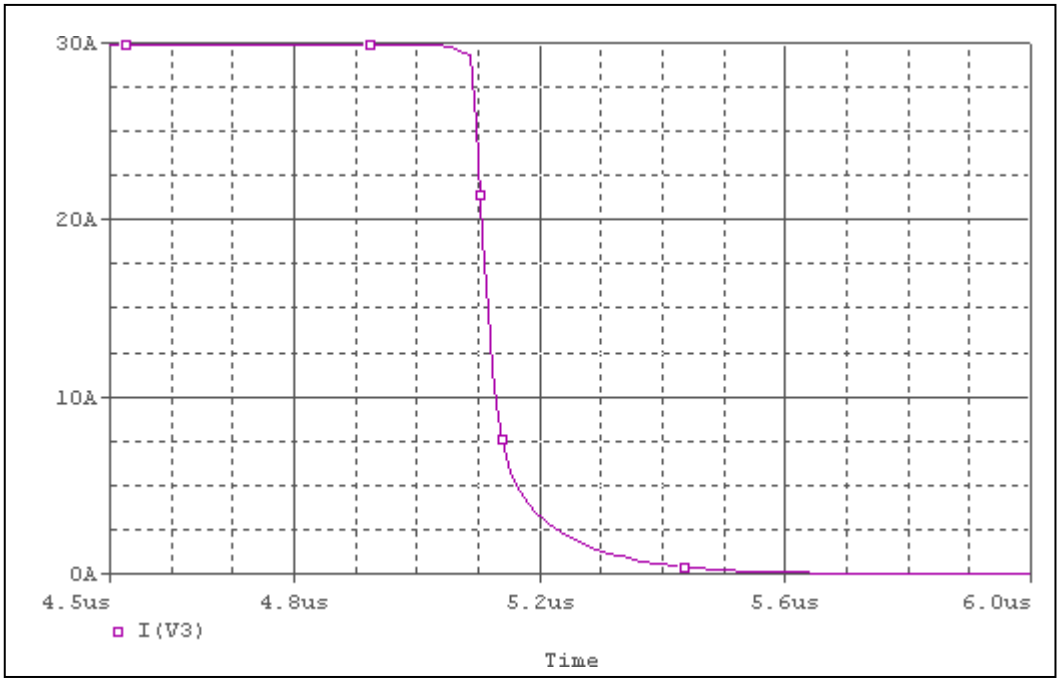
Simulation Result

Test condition : Vce = 10 V

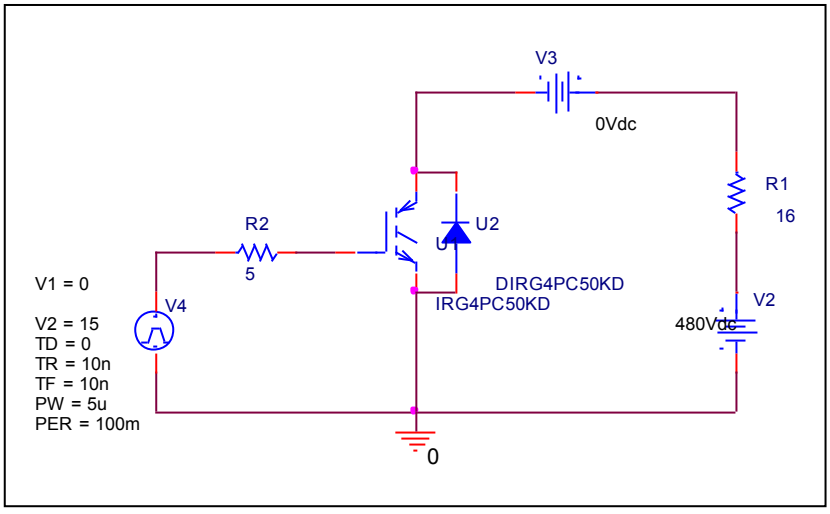
Ic(A)	Vge(V)		Error (%)
	Measurement	Simulation	
1	7	7.0434	0.62000
2	7.23	7.2251	-0.06777
5	7.62	7.5851	-0.45801
10	8.02	8.00	-0.24938
20	8.55	8.5794	0.34386

Fall Time Characteristics

Circuit Simulation result



Evaluation circuit

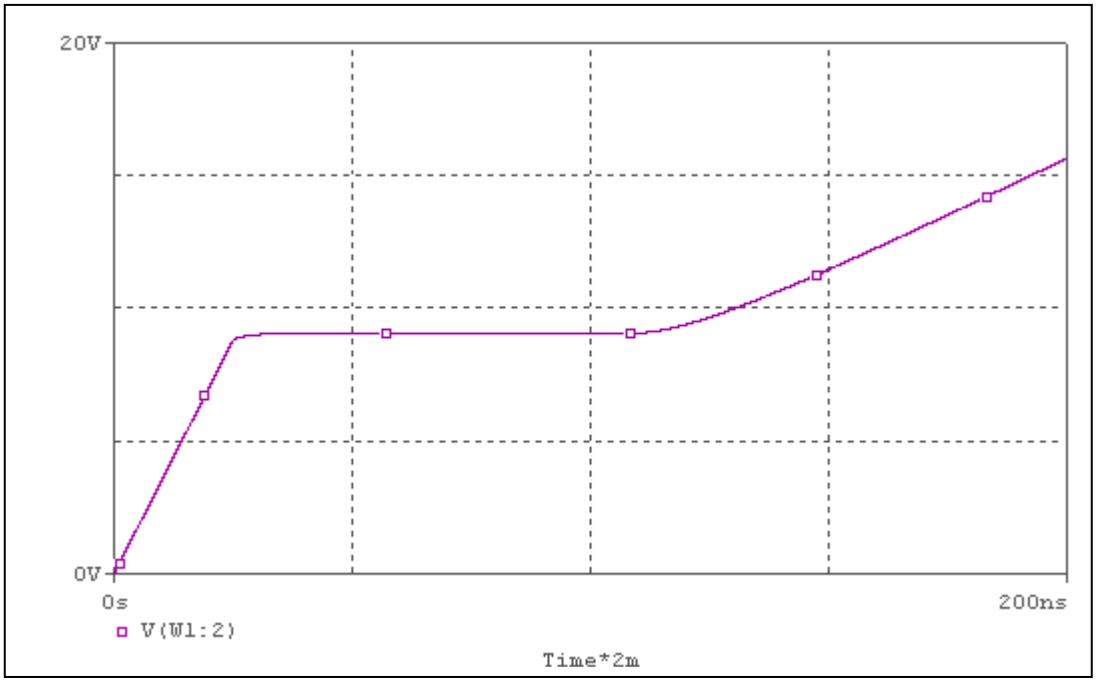


Test condition Ic=30(A) ,Vcc=480(V)

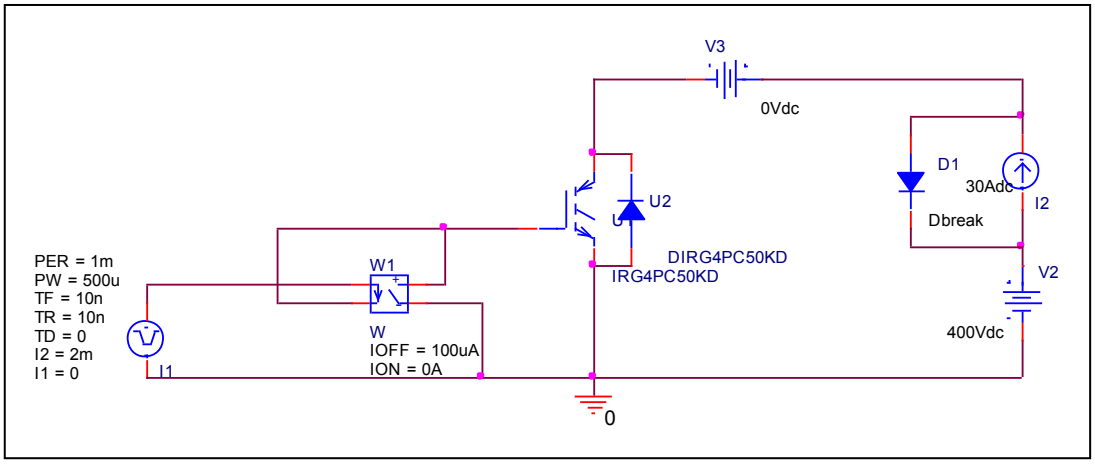
tf	Measurement		Simulation	
	95[Typ.]~140[Max.]	ns	112.790	ns

Gate Charge Characteristics

Circuit Simulation result



Evaluation circuit

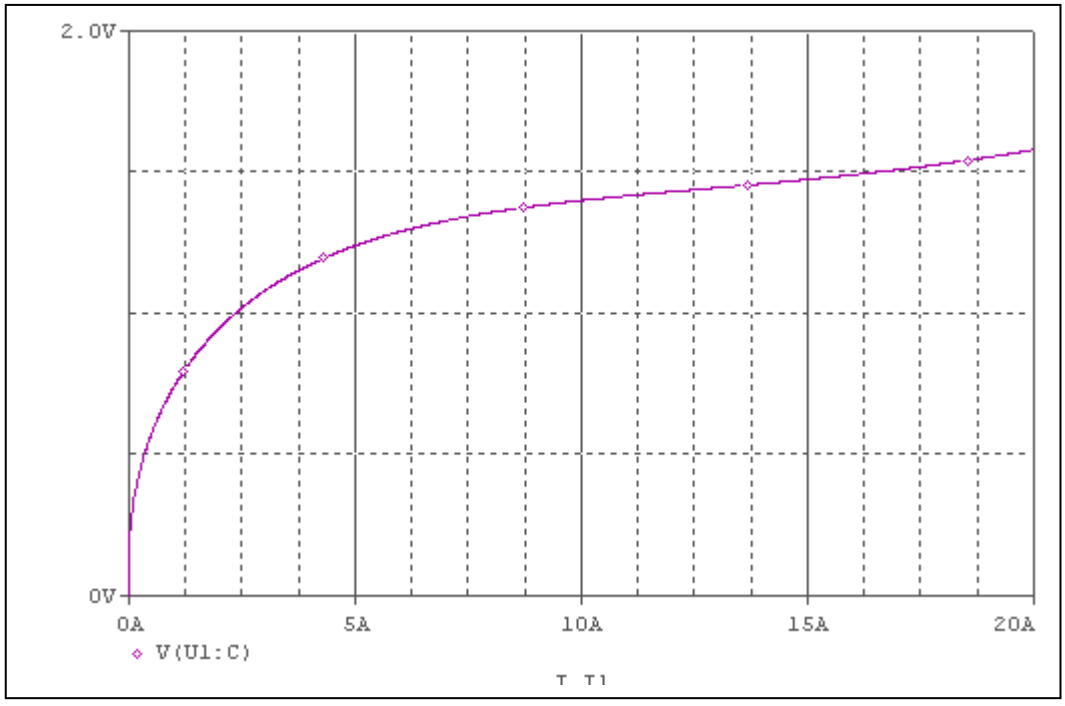


Test condition : Vcc=400(V) ,Ic=30(A) ,Vge=14(V)

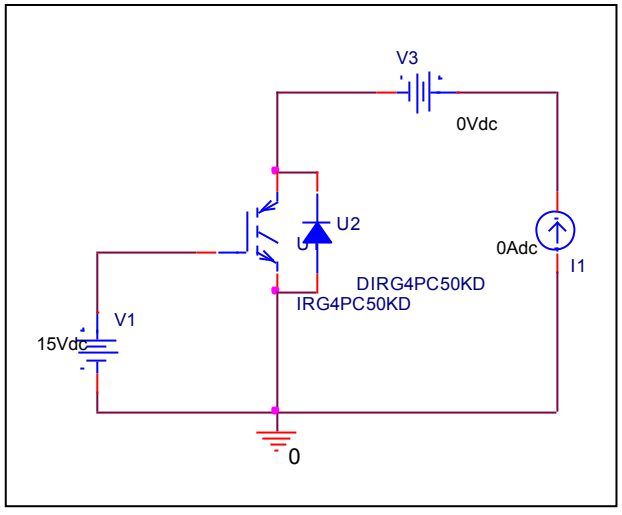
	Measurement		Simulation		Error(%)
Qge	25	nc	25.2785	nc	1.11400
Qgc	85	nc	87.253	nc	2.65059
Qg	182	nc	180.659	nc	-0.73681

Saturation Characteristics

Circuit Simulation result

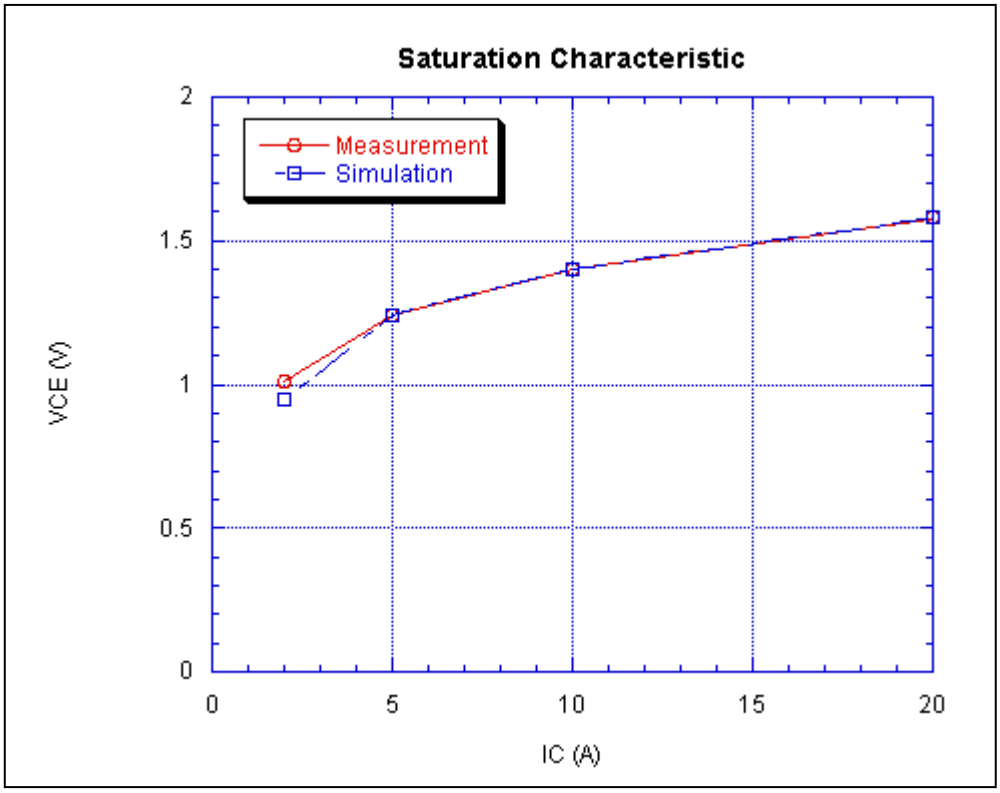


Evaluation circuit



Comparison Graph

Circuit Simulation Result

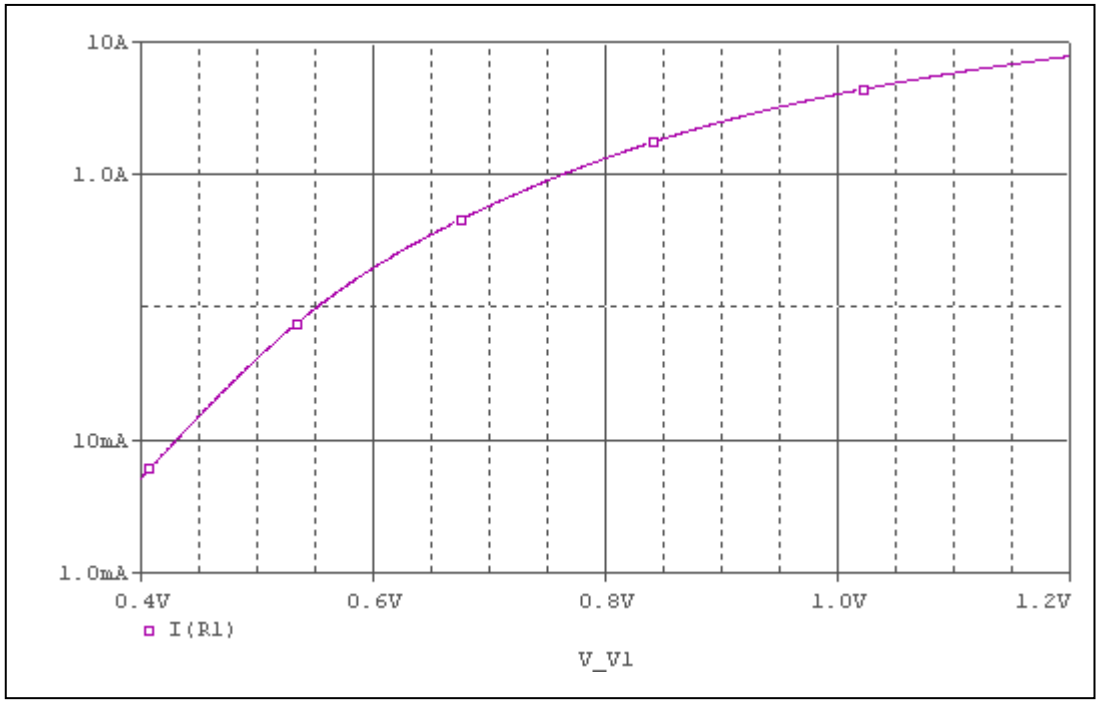


Simulation Result

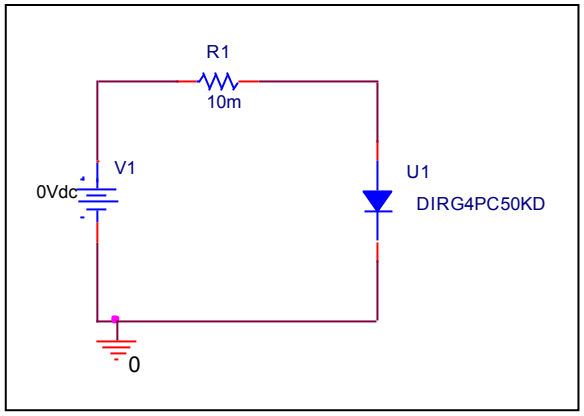
Ic(A)	Vce(sat)(V)		Error (%)
	Measurement	Simulation	
2	1.01	0.948462	-6.09287
5	1.24	1.2406	0.04839
10	1.40	1.3998	-0.01429
20	1.58	1.5800	0.00000

Forward Current Characteristic

Circuit Simulation Result

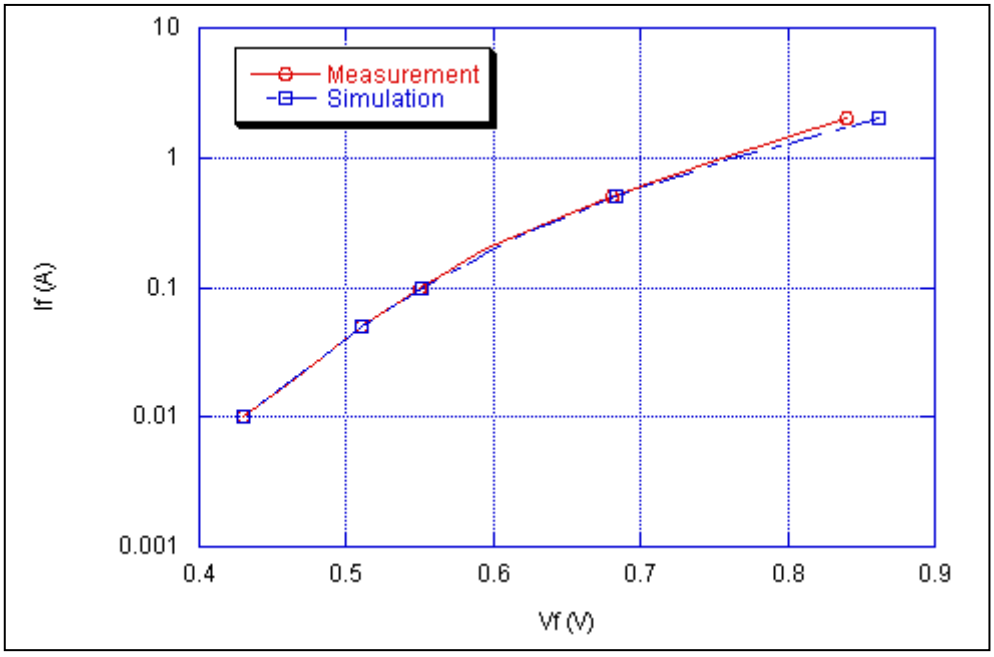


Evaluation circuit



Circuit Simulation Result

Comparison graph

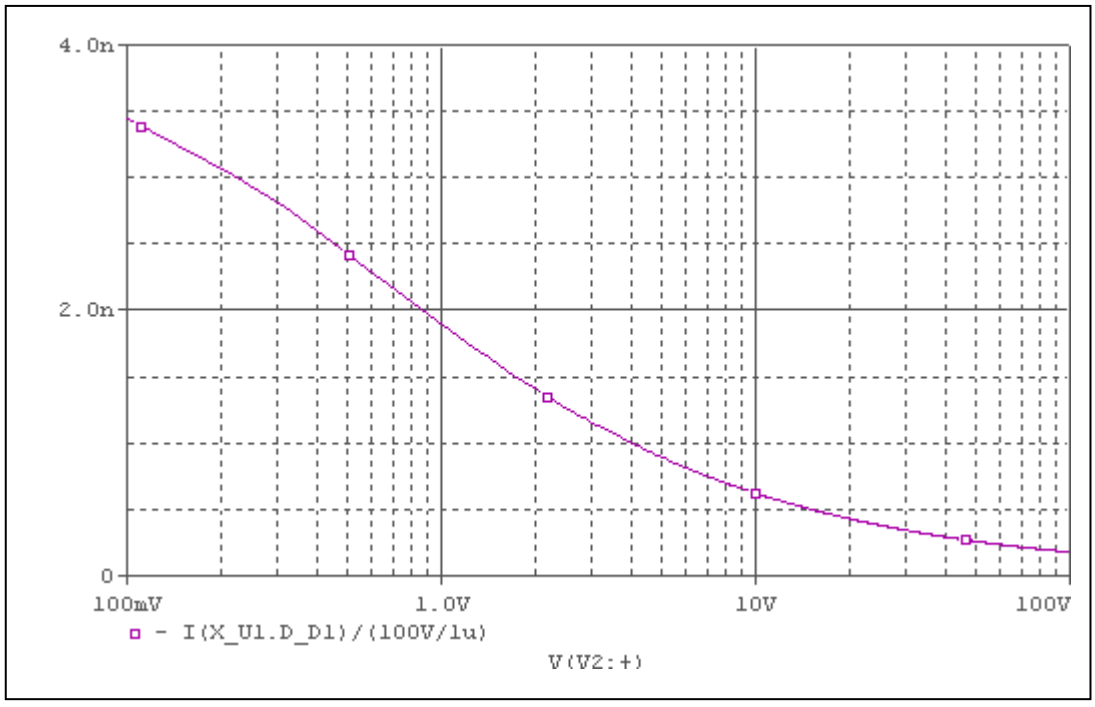


Simulation Result

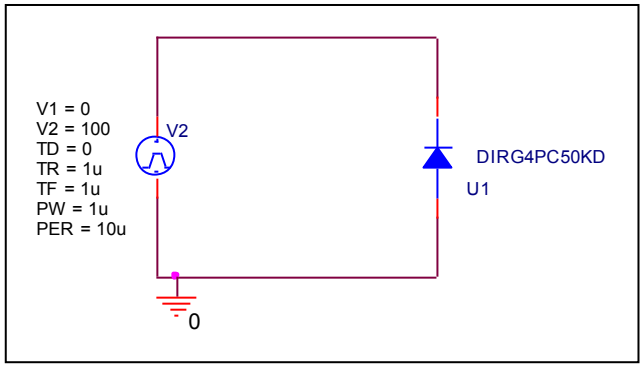
Ifwd (A)	Vfwd(V) Measurement	Vfwd(V) Simulation	%Error
0.01	0.43	0.43072	0.16744
0.02	0.465	0.463218	-0.38323
0.05	0.51	0.510821	0.16098
0.1	0.55	0.551433	0.26055
0.2	0.595	0.600523	0.92824
0.5	0.68	0.684186	0.61559
1	0.755	0.763061	1.06768
2	0.84	0.861770	2.59167

Junction Capacitance Characteristic

Circuit Simulation Result

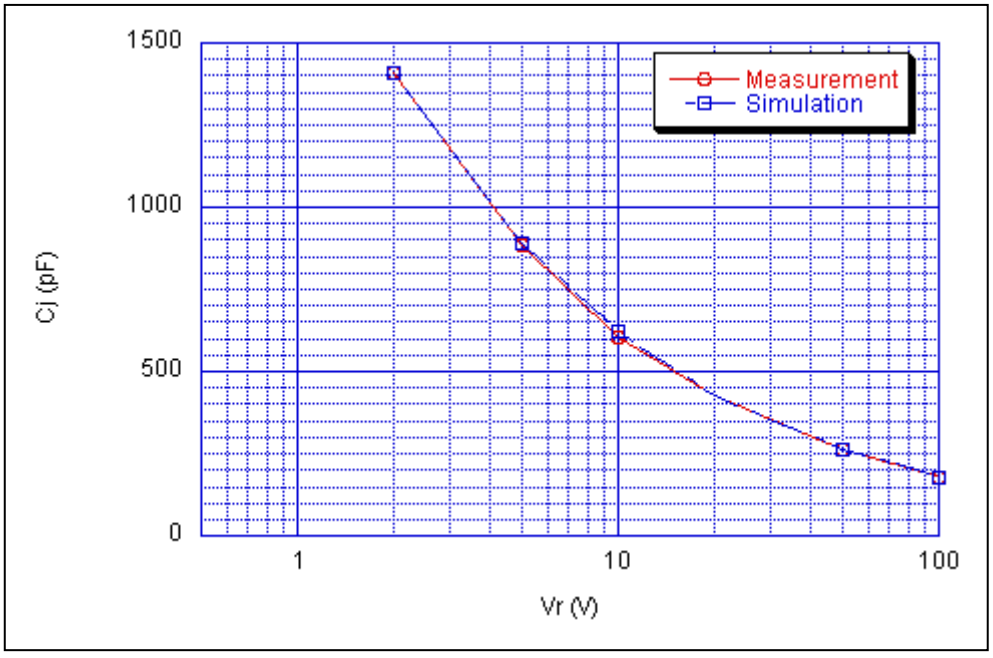


Evaluation circuit



Circuit Simulation Result

Comparison graph

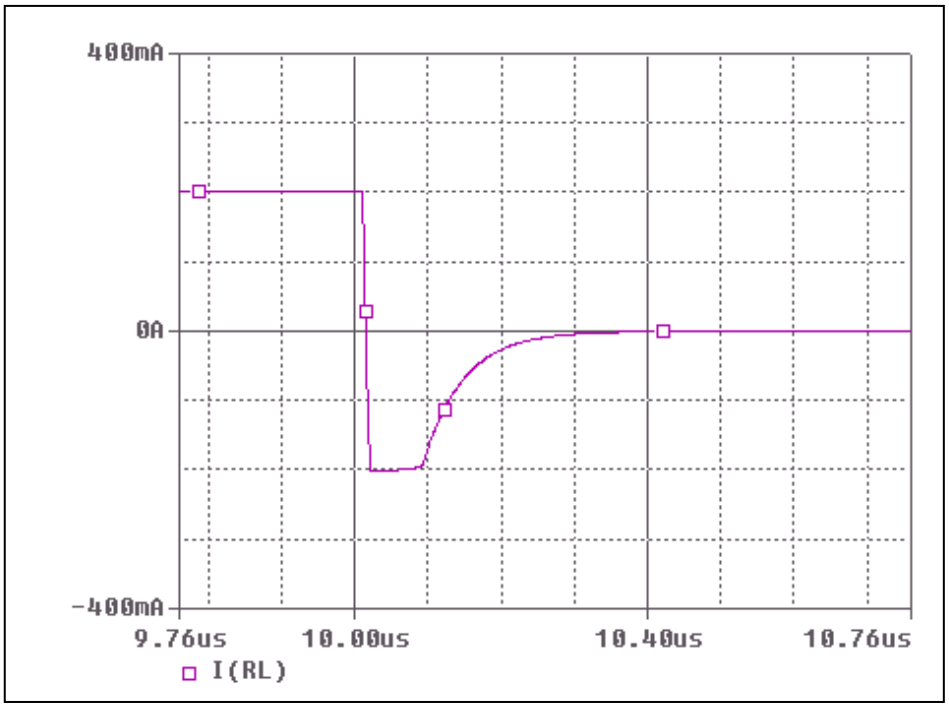


Simulation Result

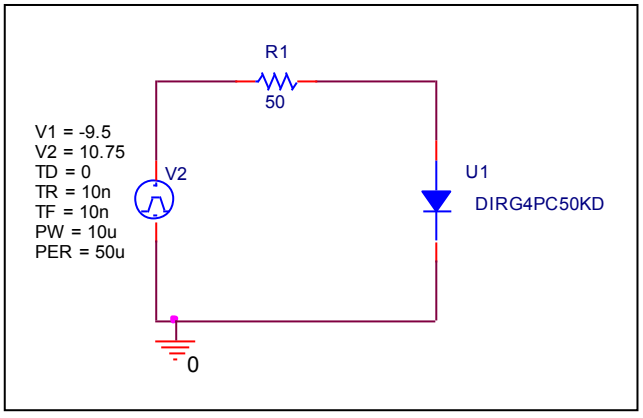
Vrev (V)	Cj(pF) Measurement	Cj(pF) Simulation	%Error
2	1409.8	1405.2	-0.32629
5	883.66	892.436	0.99314
10	604.62	621.149	2.73378
20	426.25	429.554	0.77513
50	264.96	259.686	-1.99049
100	177.89	177.871	-0.01068

Reverse Recovery Characteristic

Circuit Simulation Result



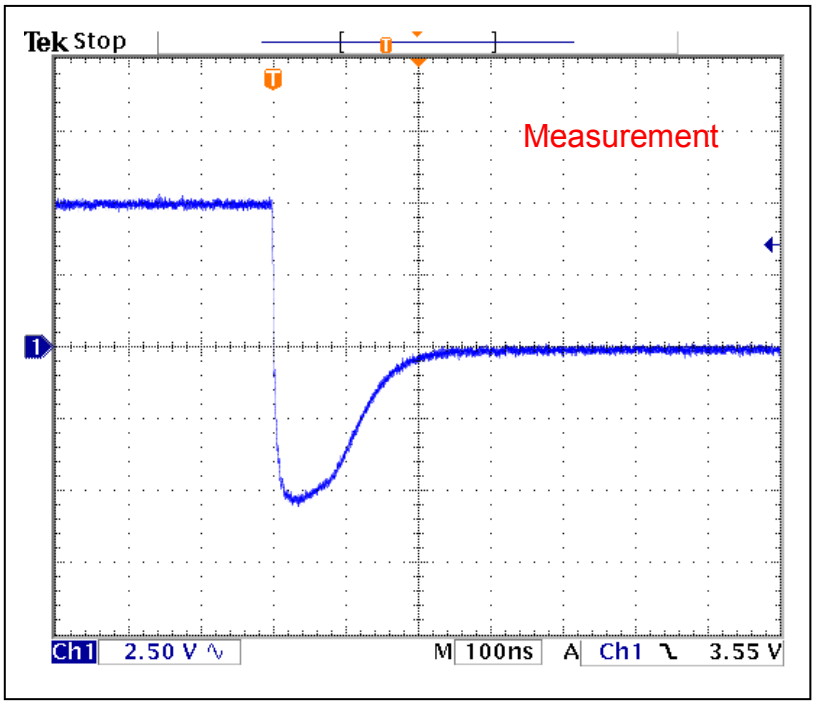
Evaluation circuit



Compare Measurement vs. Simulation

	Measurement		Simulation		Error(%)
trj	64	ns	64.335	ns	0.52344
trb	136	ns	135.78	ns	-0.16176

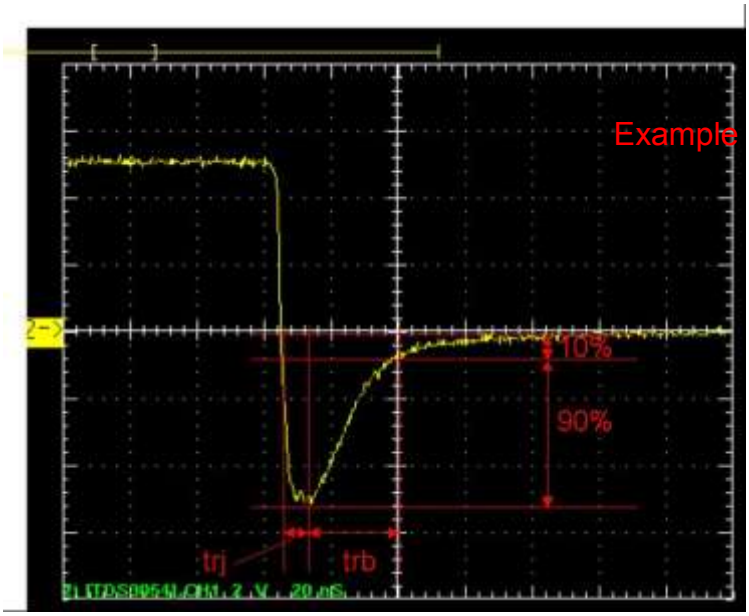
Reverse Recovery Characteristic Reference



trj=64(ns)

trb=136(ns)

Conditions:Ifwd=Irev=0.2(A),Rl=50



Relation between trj and trb