# Device Modeling Report

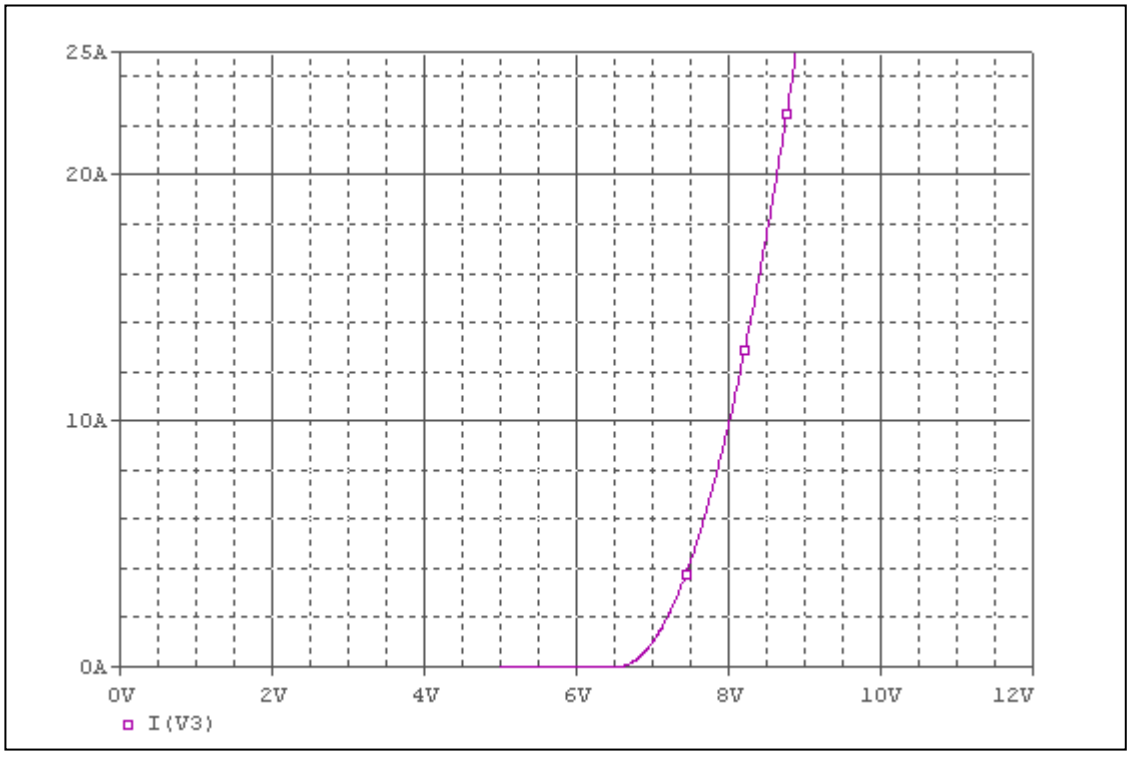
COMPONENTS: Insulated Gate Bipolar Transistor (IGBT)
PART NUMBER: IRG4PH50KD
MANUFACTURER: International Rectifier


**Bee Technologies Inc.**

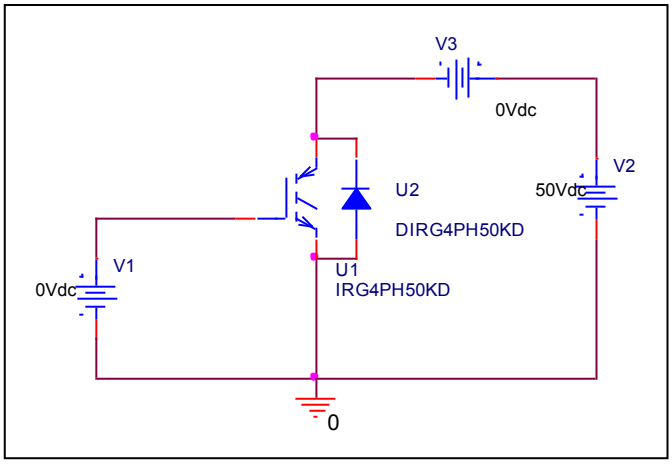
| Pspice model parameter | Model description |
|---|---|
| TAU | Ambipolar Recombination Lifetime |
| KP | MOS Transconductance |
| AREA | Area of the Device |
| AGD | Gate-Drain Overlap Area |
| WB | Metallurgical Base Width |
| VT | Threshold Voltage |
| KF | Triode Region Factor |
| CGS | Gate-Source Capacitance per Unit Area |
| COXD | Gate-Drain Oxide Capacitance per Unit Area |
| VTD | Gate-Drain Overlap Depletion Threshold |

## Transfer Characteristics

Circuit Simulation result

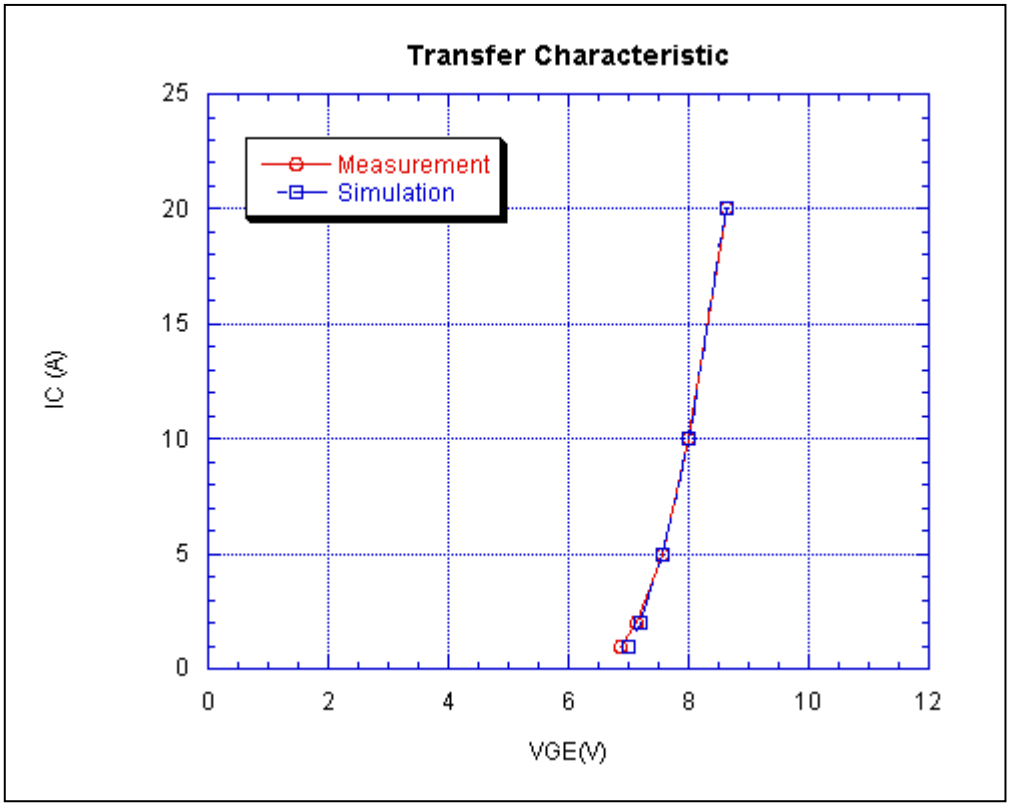



Evaluation circuit



## Comparison Graph

Circuit Simulation Result



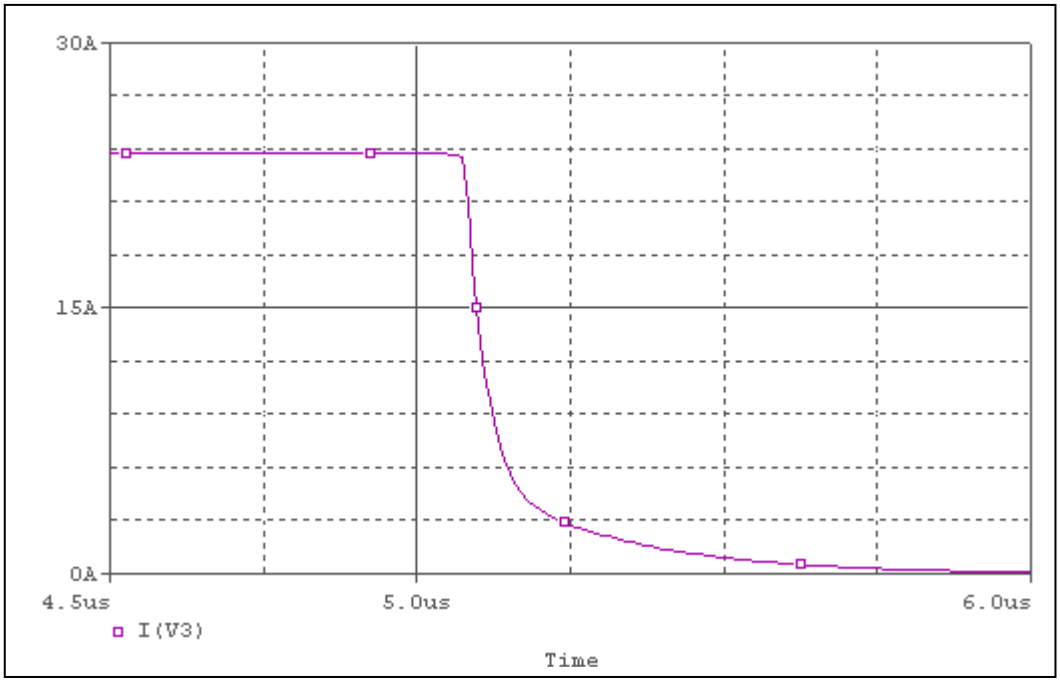

Simulation Result

**Test condition : Vce = 10 V**

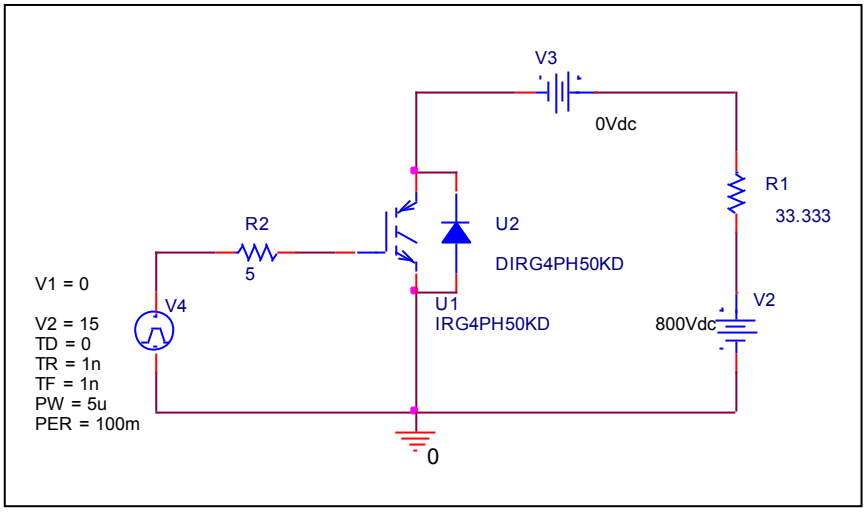
| Ic(A) | Vge(V) | | Error (%) |
|---|---|---|---|
| | Measurement | Simulation | |
| 1 | 6.88 | 7 | 1.74419 |
| 2 | 7.13 | 7.1892 | 0.83029 |
| 5 | 7.57 | 7.5811 | 0.14663 |
| 10 | 8.01 | 8.0134 | 0.04245 |
| 20 | 8.62 | 8.6371 | 0.19838 |

## Fall Time Characteristics

Circuit Simulation result




Evaluation circuit

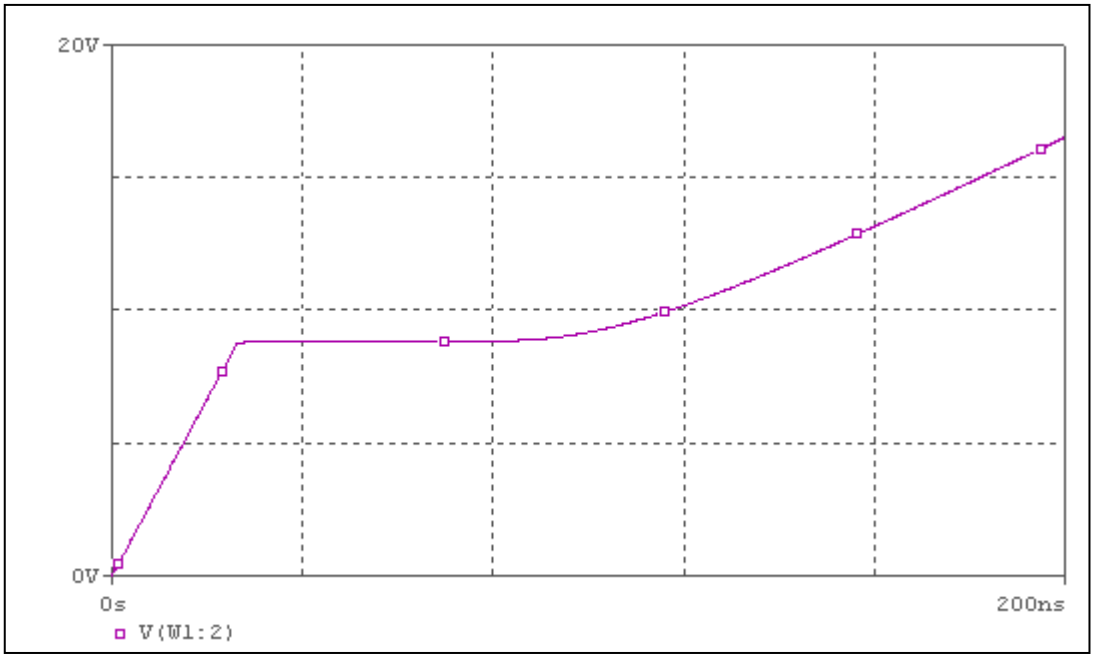



Test condition Ic=24(A) ,Vcc=800(V)

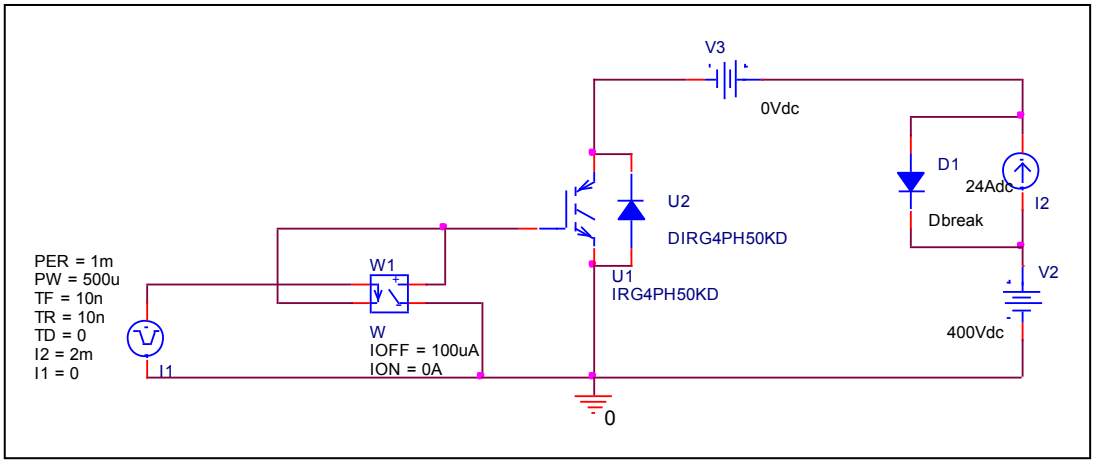
| tf | Measurement | | Simulation | | Error |
|---|---|---|---|---|---|
| | 200 | ns | 201.940 | ns | 0.97000 |

## Gate Charge Characteristics

Circuit Simulation result




Evaluation circuit

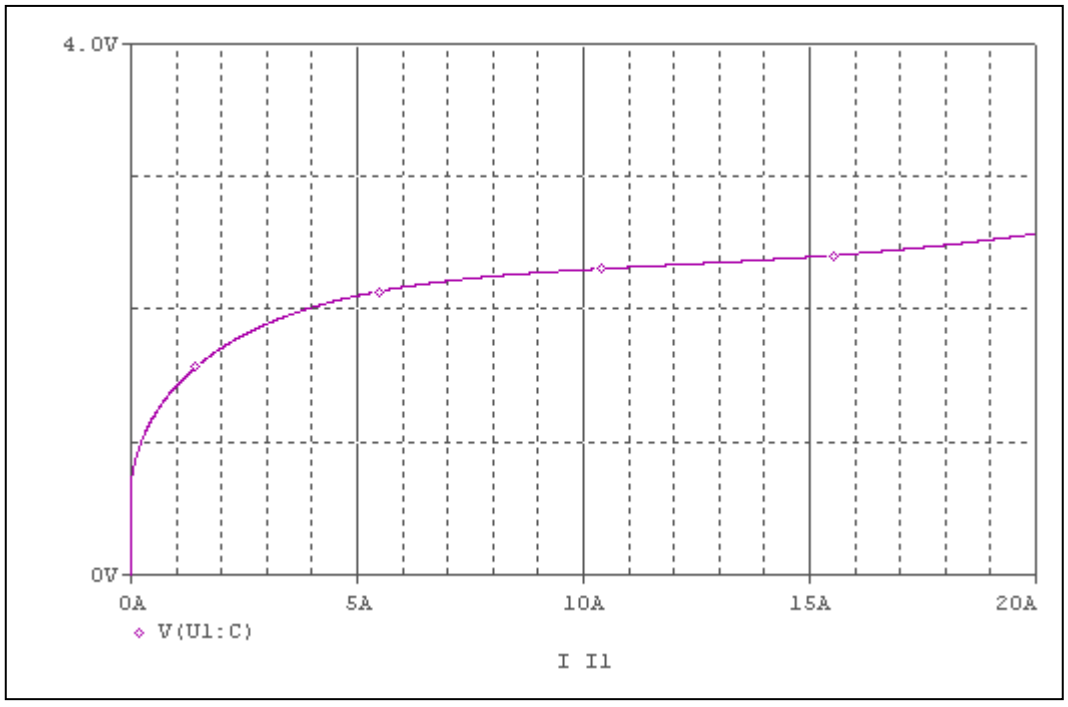



Test condition : Vcc=400(V) ,Ic=24(A) ,Vge=14.8(V)

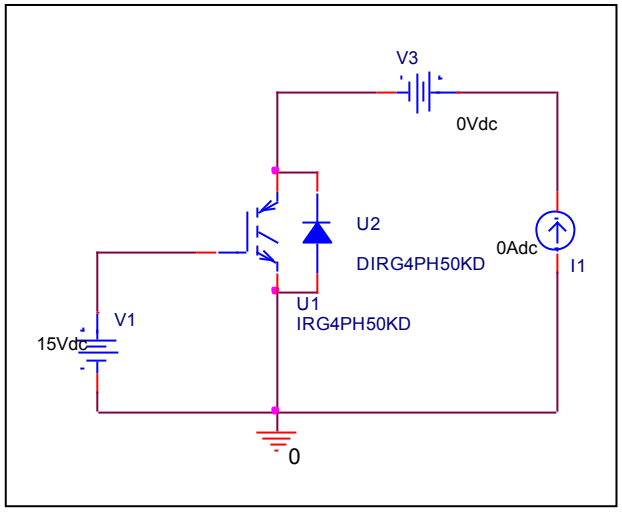
| | Measurement | | Simulation | | Error(%) |
|---|---|---|---|---|---|
| Qge | 26 | nc | 26.374 | nc | 1.43846 |
| Qgc | 70 | nc | 68.132 | nc | -2.66857 |
| Qg | 180 | nc | 179.780 | nc | -0.12222 |

## Saturation Characteristics

Circuit Simulation result

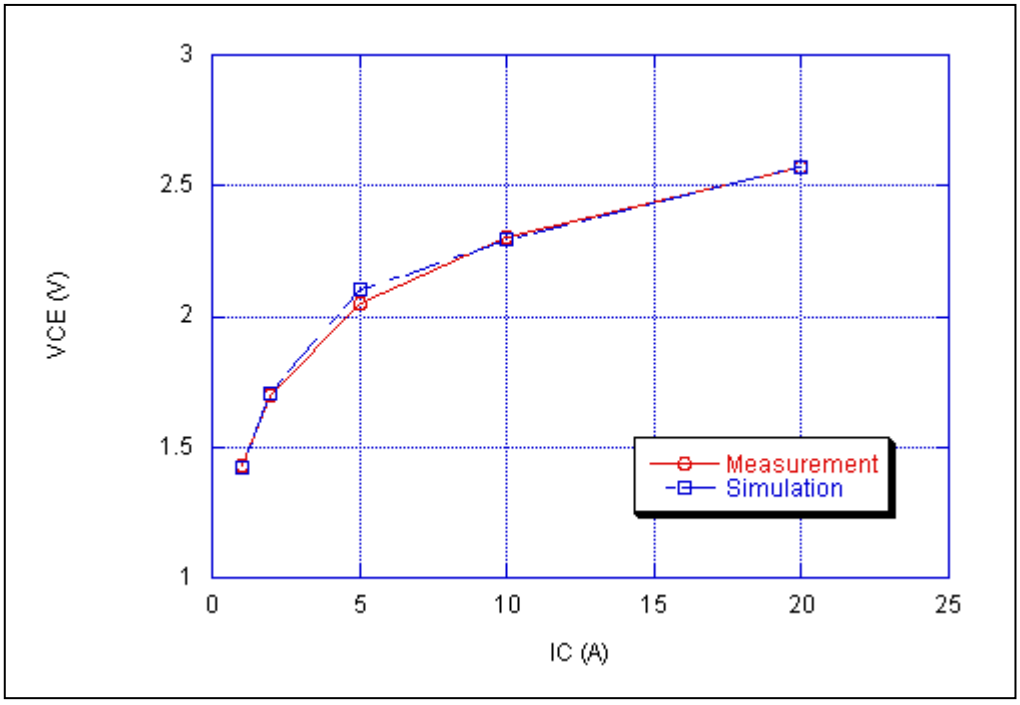



Evaluation circuit



## Comparison Graph

Circuit Simulation Result

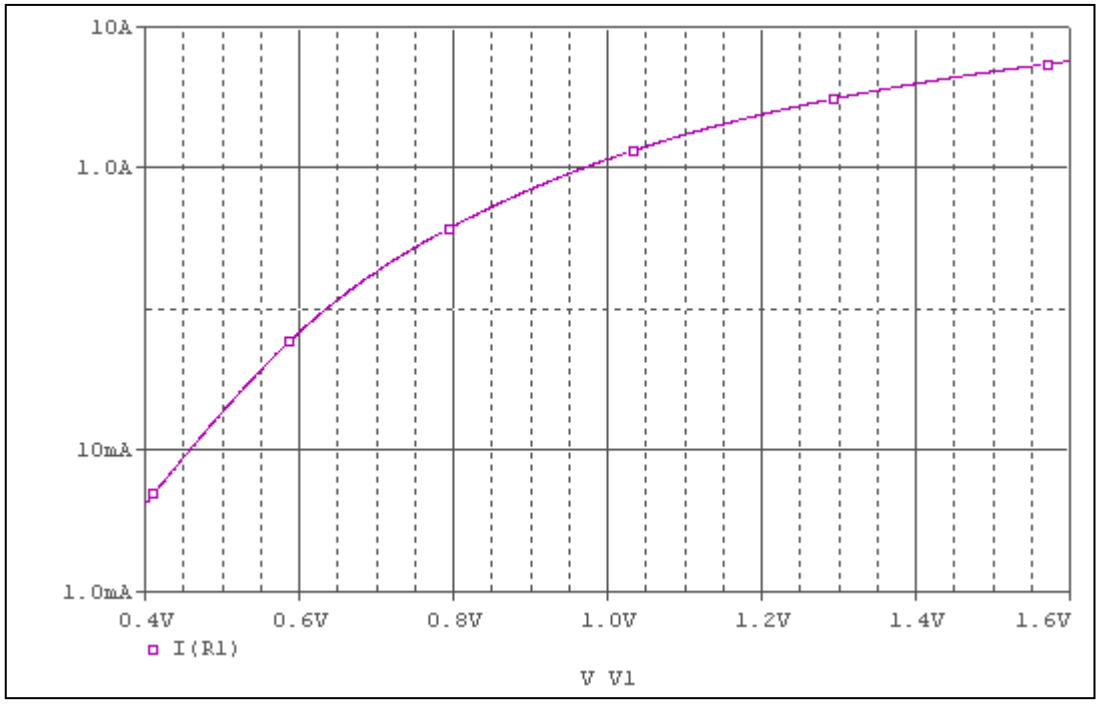



Simulation Result

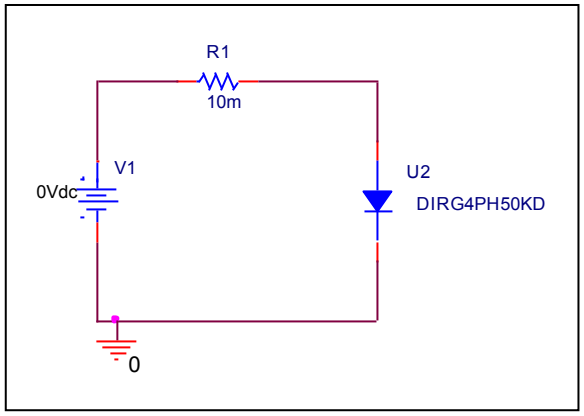
| Ic(A) | Vce(sat)(V) | | Error (%) |
|---|---|---|---|
| | Measurement | Simulation | |
| 1 | 1.43 | 1.4270 | -0.20979 |
| 2 | 1.7 | 1.7130 | 0.76471 |
| 5 | 2.05 | 2.1036 | 2.61463 |
| 10 | 2.3 | 2.2984 | -0.06957 |
| 20 | 2.57 | 2.5704 | 0.01556 |

## Forward Current Characteristic

Circuit Simulation Result

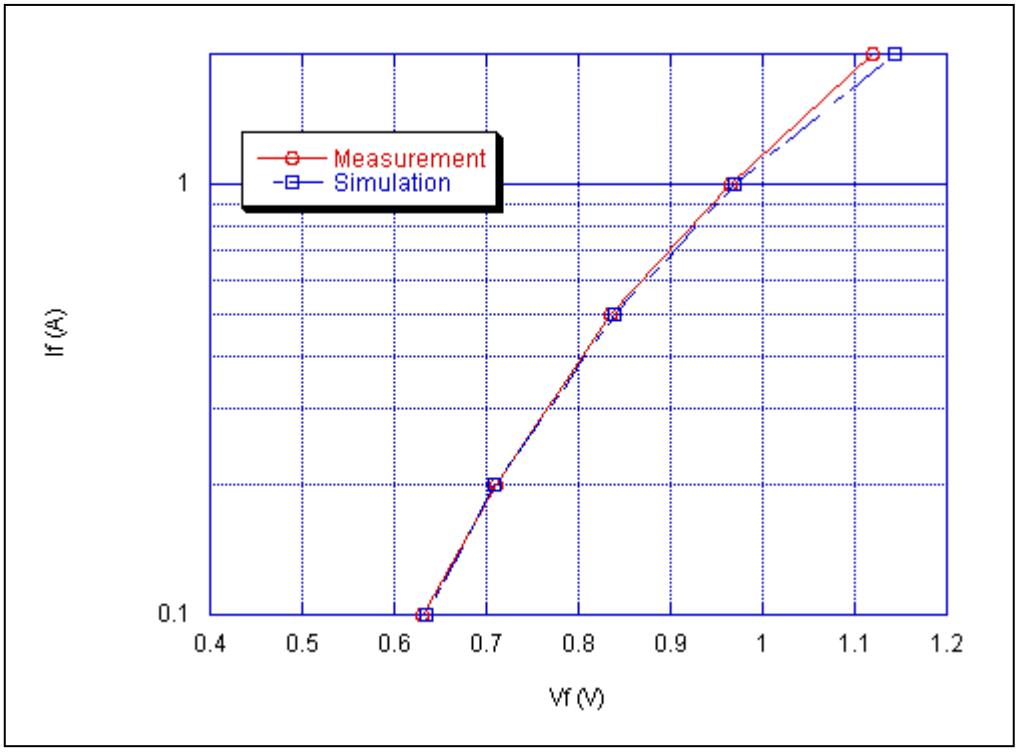



Evaluation circuit



Circuit Simulation Result

## Comparison graph

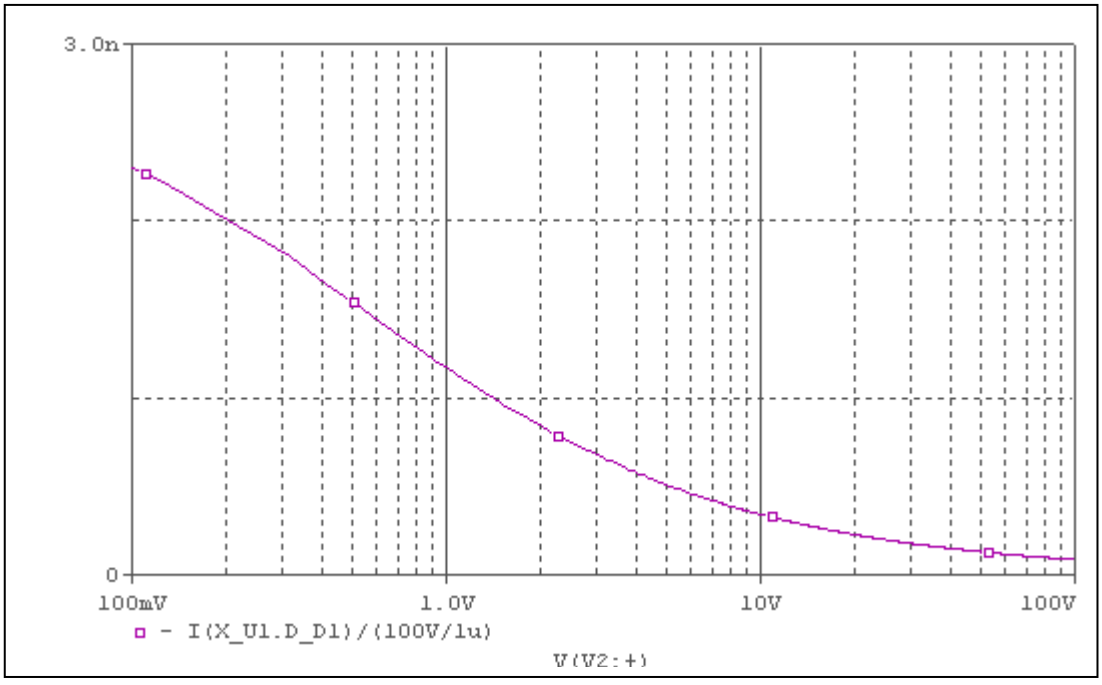



## Simulation Result

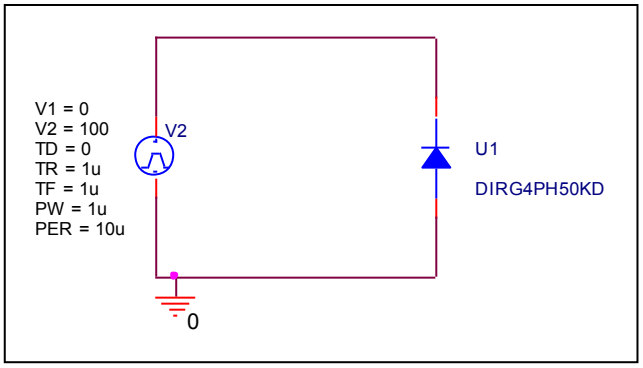
| Ifwd (A) | Vfwd(V) Measurement | Vfwd(V) Simulation | %Error |
|---|---|---|---|
| 0.1 | 0.63 | 0.637257 | 1.15190 |
| 0.2 | 0.71 | 0.710151 | 0.02127 |
| 0.5 | 0.835 | 0.839306 | 0.51569 |
| 1 | 0.965 | 0.966942 | 0.20124 |
| 2 | 1.12 | 1.1437 | 2.11607 |

## Junction Capacitance Characteristic

Circuit Simulation Result

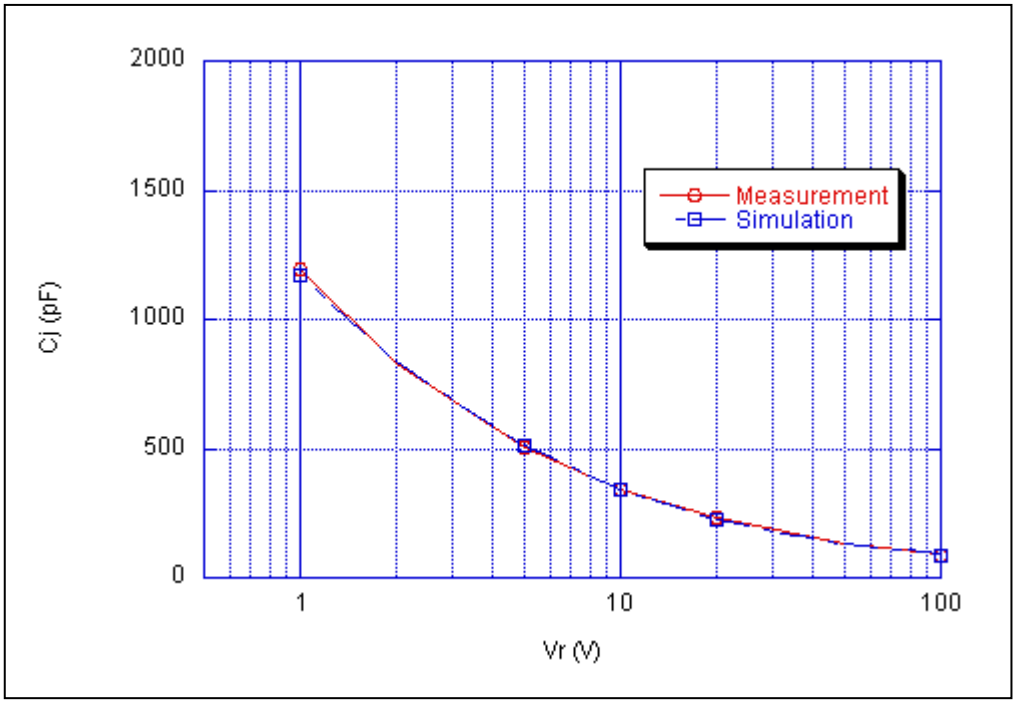



Evaluation circuit



Circuit Simulation Result

## Comparison graph

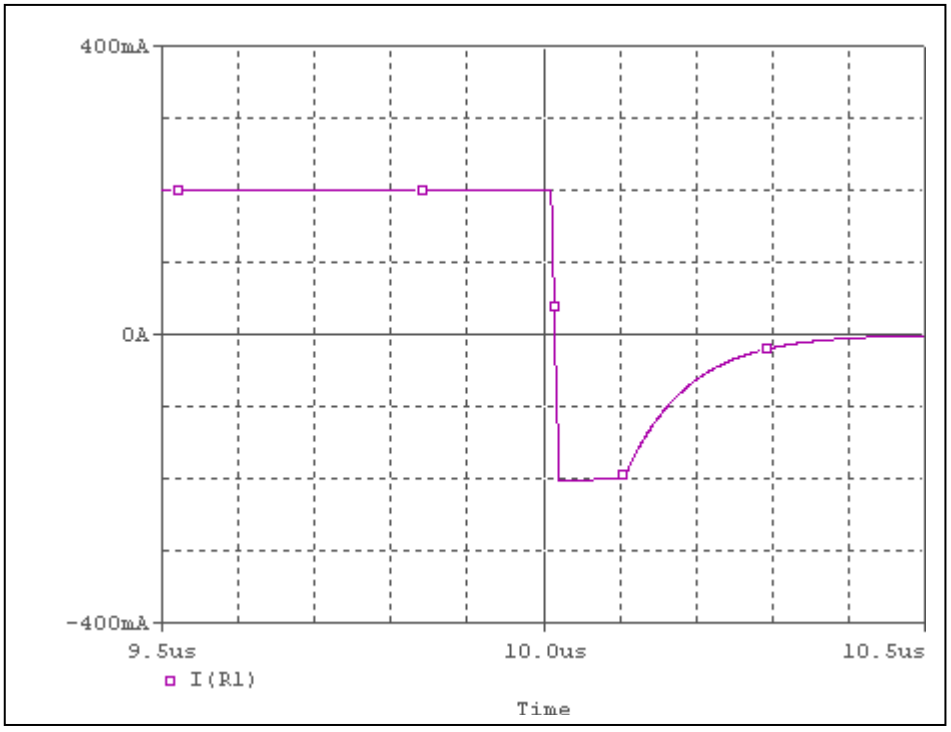



Simulation Result

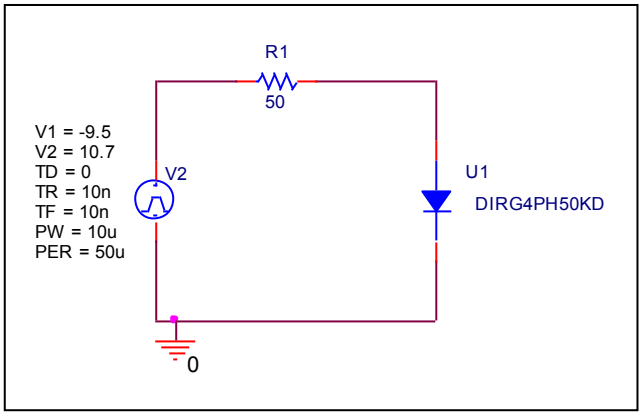
| Vrev (V) | Cj(pF) Measurement | Cj(pF) Simulation | %Error |
|---|---|---|---|
| 1 | 1196.2 | 1171.1 | -2.09831 |
| 2 | 832.23 | 838.131 | 0.70906 |
| 5 | 504 | 509.306 | 1.05278 |
| 10 | 341.12 | 340.999 | -0.03547 |
| 20 | 230.67 | 226.595 | -1.76659 |
| 50 | 132.56 | 130.224 | -1.76222 |
| 100 | 87.6 | 85.665 | -2.20890 |

## Reverse Recovery Characteristic

Circuit Simulation Result




Evaluation circuit

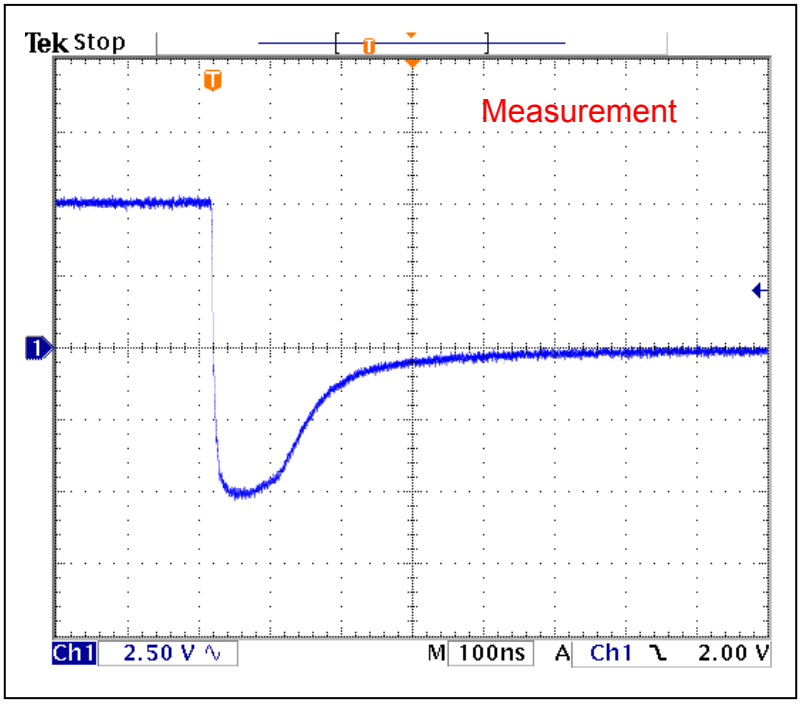



Compare Measurement vs. Simulation

| | Measurement | | Simulation | | Error(%) |
|---|---|---|---|---|---|
| trj | 78 | ns | 78.107 | ns | 0.137 |
| trb | 200 | ns | 200.23 | ns | 0.115 |

## Reverse Recovery Characteristic

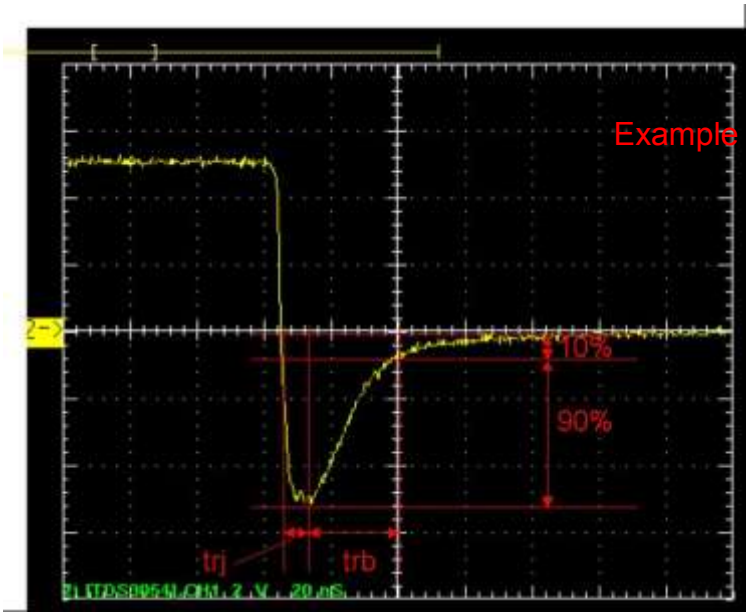
**Reference**




trj=78(ns)

trb=200(ns)

Conditions:Ifwd=Irev=0.2(A),Rl=50




Relation between trj and trb