Device Modeling Report

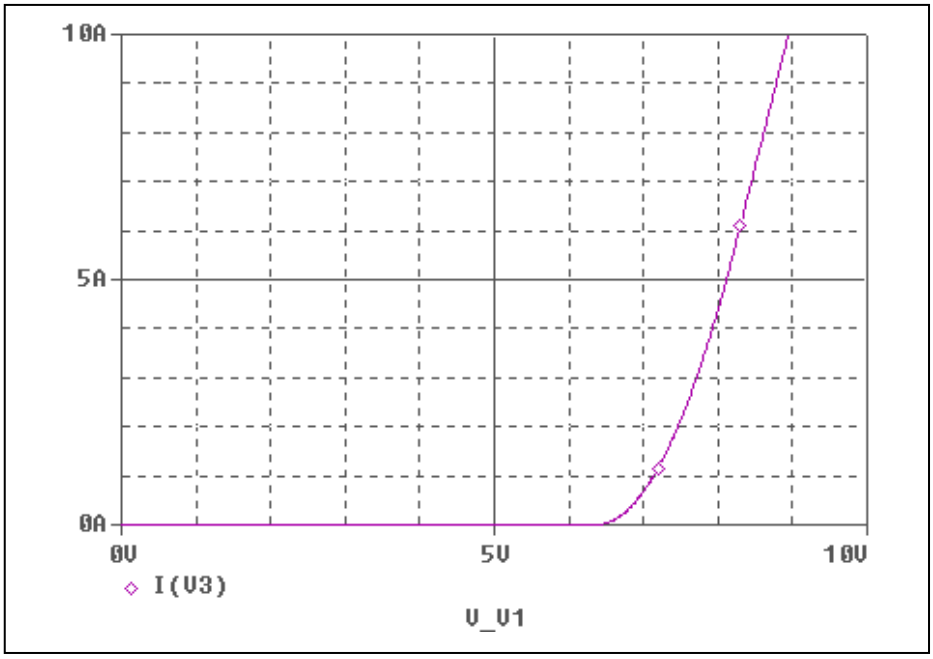
COMPONENTS: Insulated Gate Bipolar Transistor (IGBT)
PART NUMBER: GT10J321
MANUFACTURER: TOSHIBA

Bee Technologies Inc.

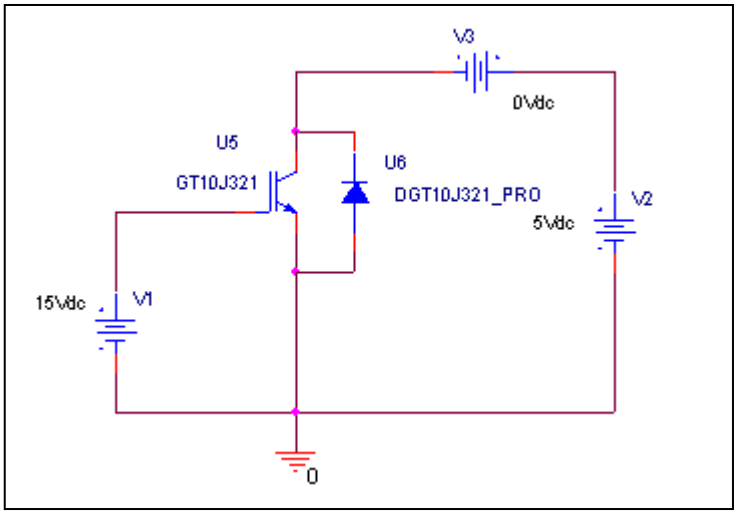
Pspice model parameter	Model description
TAU	Ambipolar Recombination Lifetime
KP	MOS Transconductance
AREA	Area of the Device
AGD	Gate-Drain Overlap Area
WB	Metallurgical Base Width
VT	Threshold Voltage
KF	Triode Region Factor
CGS	Gate-Source Capacitance per Unit Area
COXD	Gate-Drain Oxide Capacitance per Unit Area
VTD	Gate-Drain Overlap Depletion Threshold

Transfer Characteristics

Circuit Simulation result



Evaluation circuit



Comparison Graph

Circuit Simulation Result

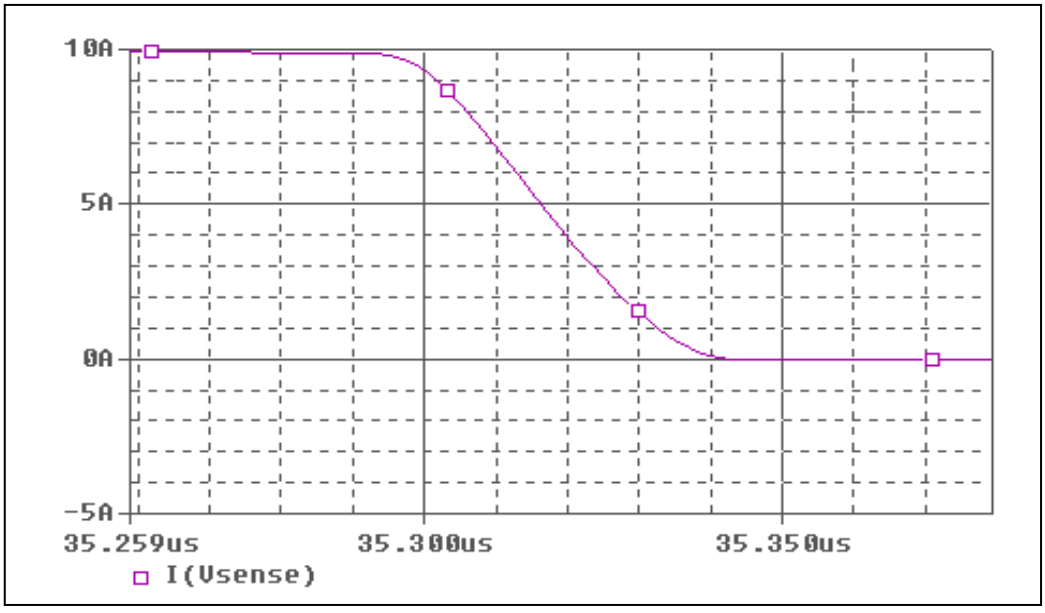
Simulation Result

Test condition : Vce = 5 V

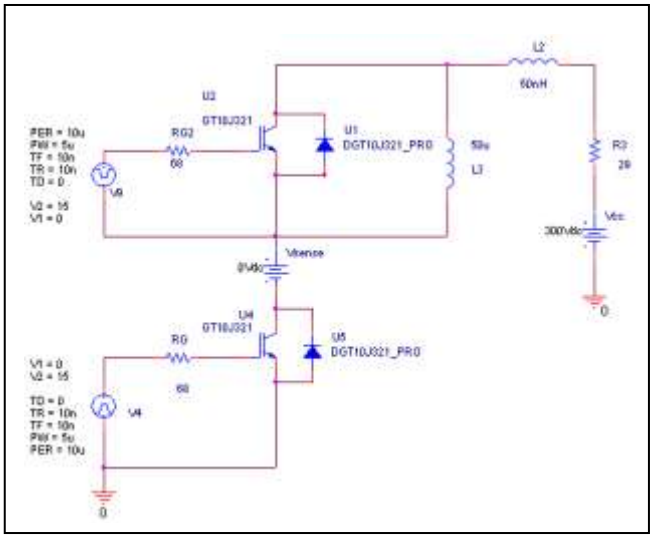
Ic(A)	Vge(V)		Error (%)
	Measurement	Simulation	
1	7.16	7.1429	-0.23883
2	7.5	7.4628	-0.49600
5	8.1	8.1142	0.17531
9	8.72	8.7814	0.70413

Fall Time Characteristics

Circuit Simulation result



Evaluation circuit

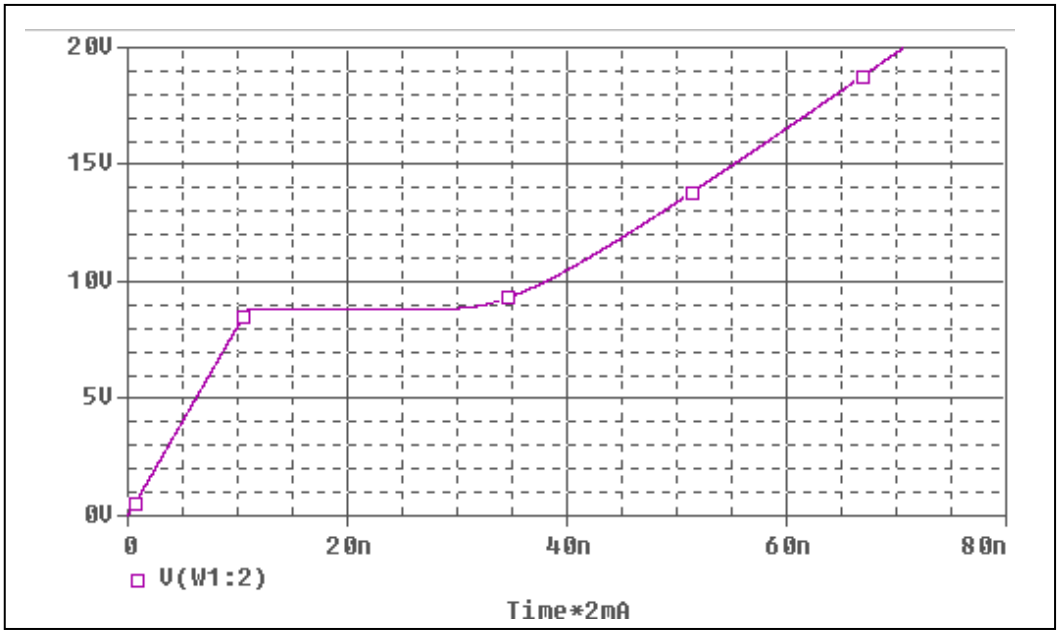


Test condition Ic=10(A) ,Vce=300(V)

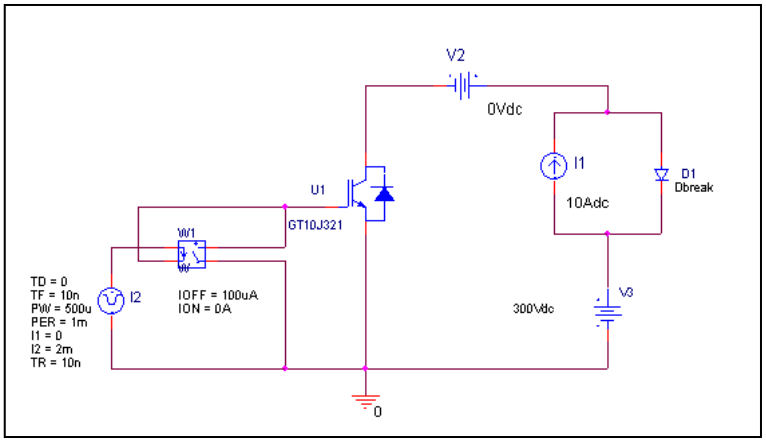
tf	Measurement		Simulation		Error
	30	ns	30.868	ns	2.893

Gate Charge Characteristics

Circuit Simulation result



Evaluation circuit

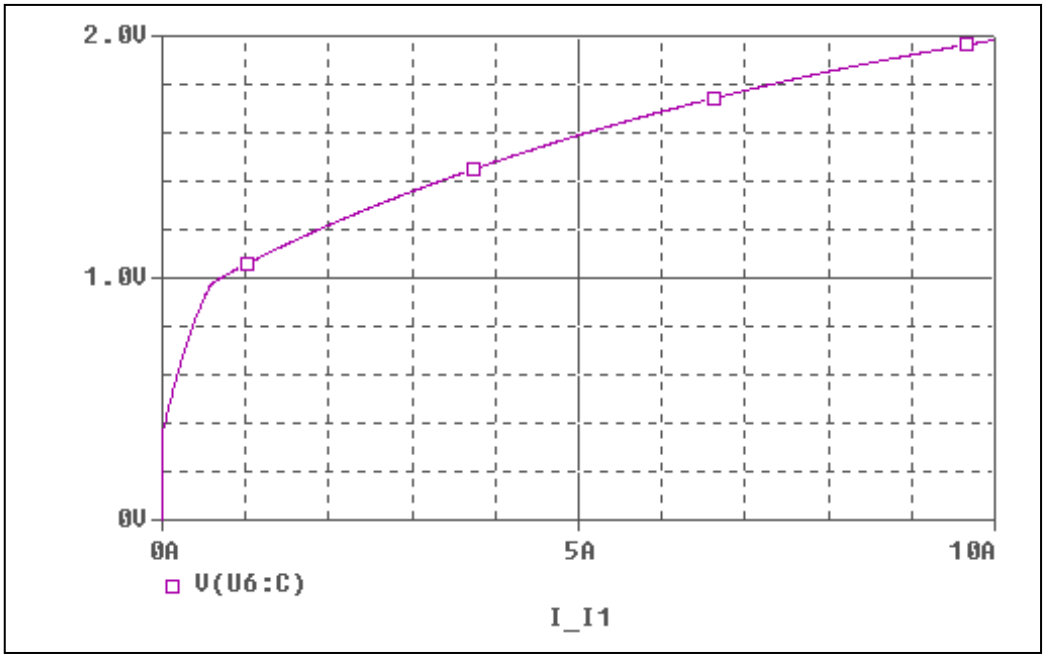


Test condition : Vcc=300(V) ,Ic=10(A) ,Vge=15(V)

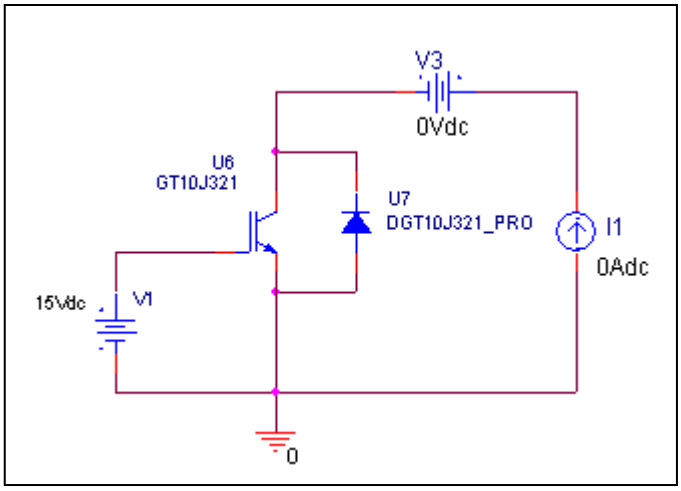
	Measurement		Simulation		Error(%)
Qge	11	nc	11.042	nc	0.38182
Qgc	20	nc	20.162	nc	0.81000
Qg	70	nc	70.625	nc	0.89286

Saturation Characteristics

Circuit Simulation result

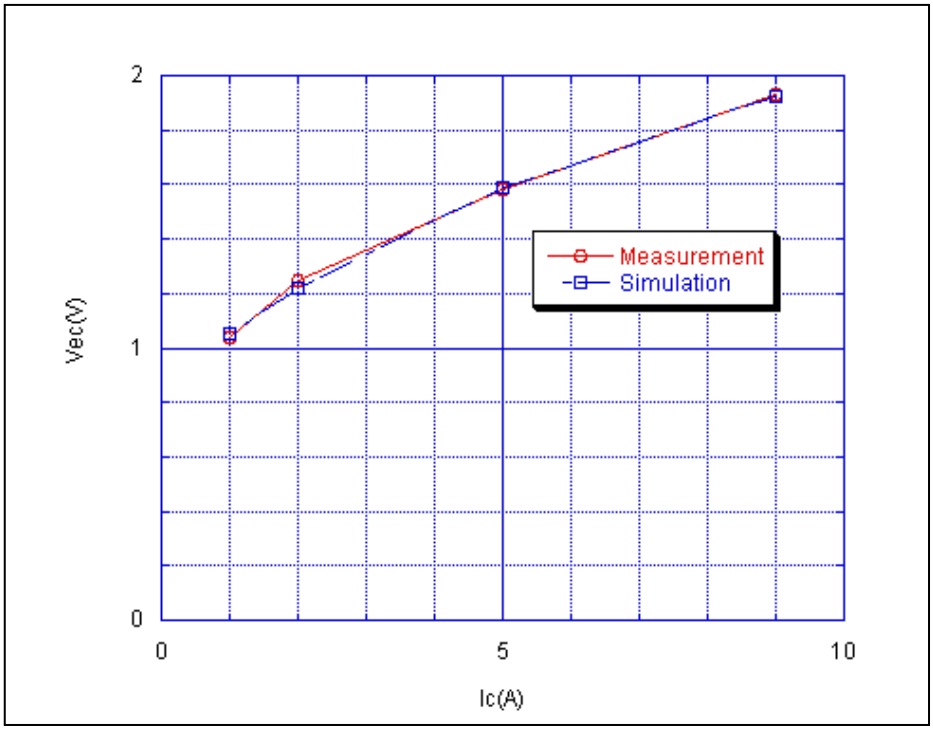


Evaluation circuit



Comparison Graph

Circuit Simulation Result

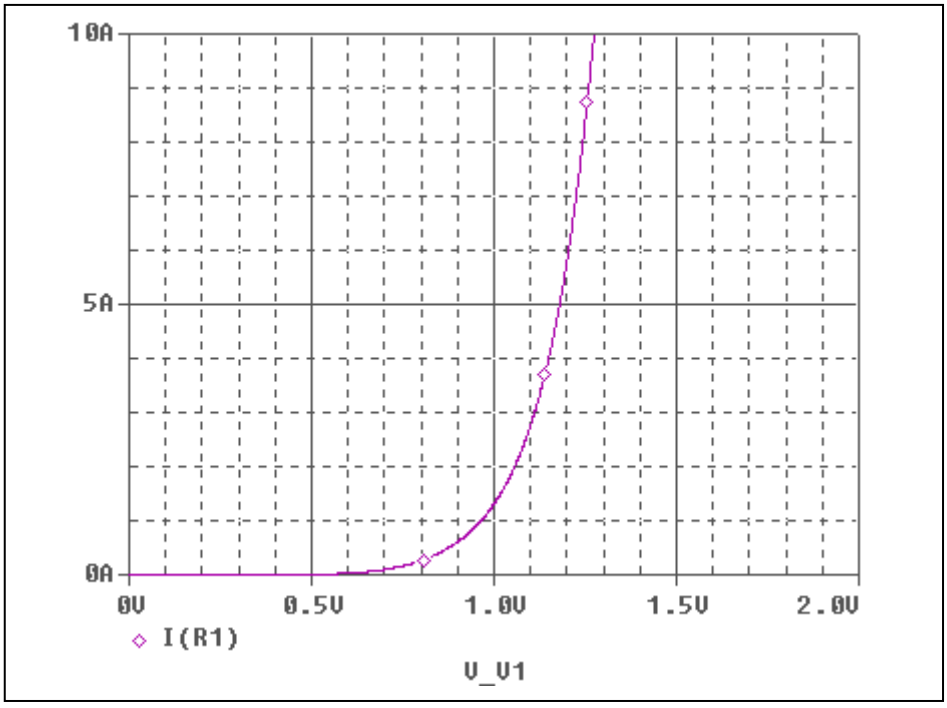


Simulation Result

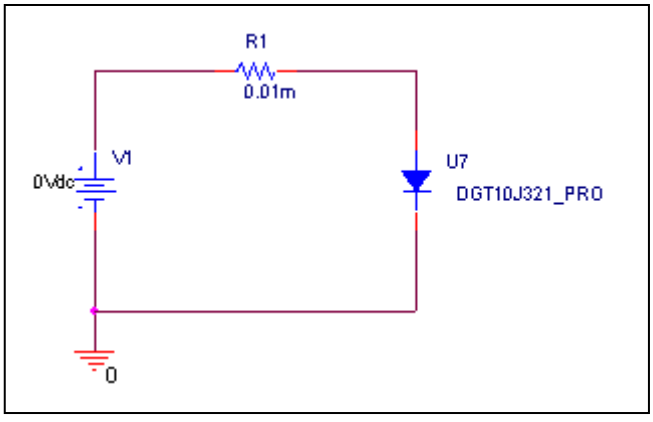
Ic(A)	Vce(sat)(V)		Error (%)
	Measurement	Simulation	
1	1.04	1.0559	1.52885
2	1.25	1.2186	-2.51200
5	1.58	1.5899	0.62658
9	1.93	1.9224	-0.39378

Forward Current Characteristic

Circuit Simulation Result

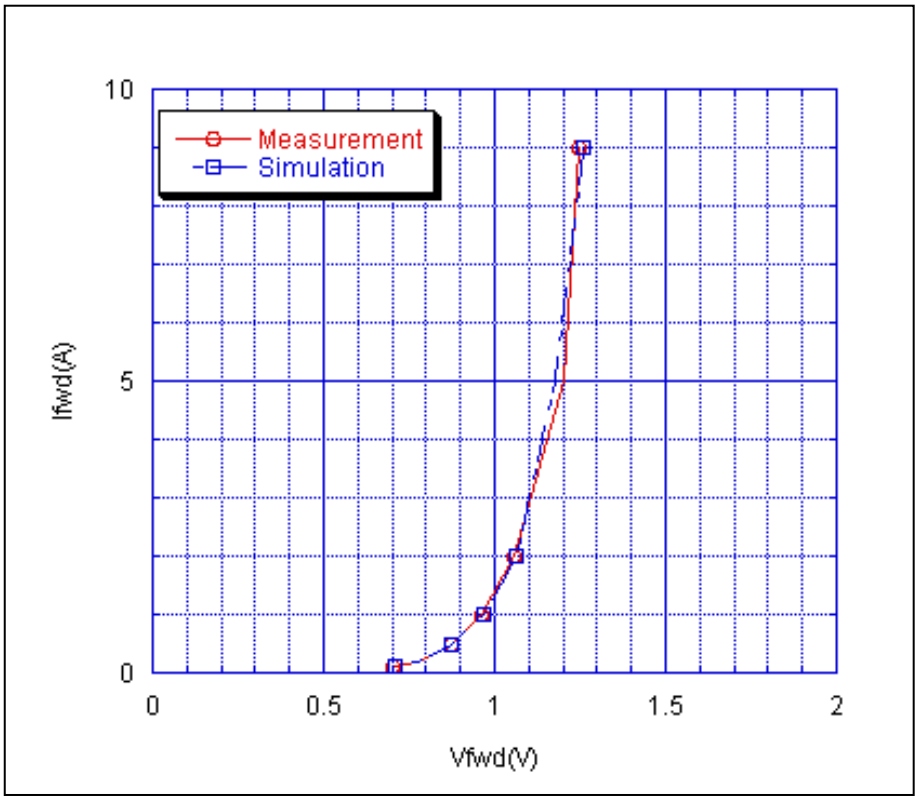


Evaluation Circuit



Comparison Graph

Circuit Simulation Result

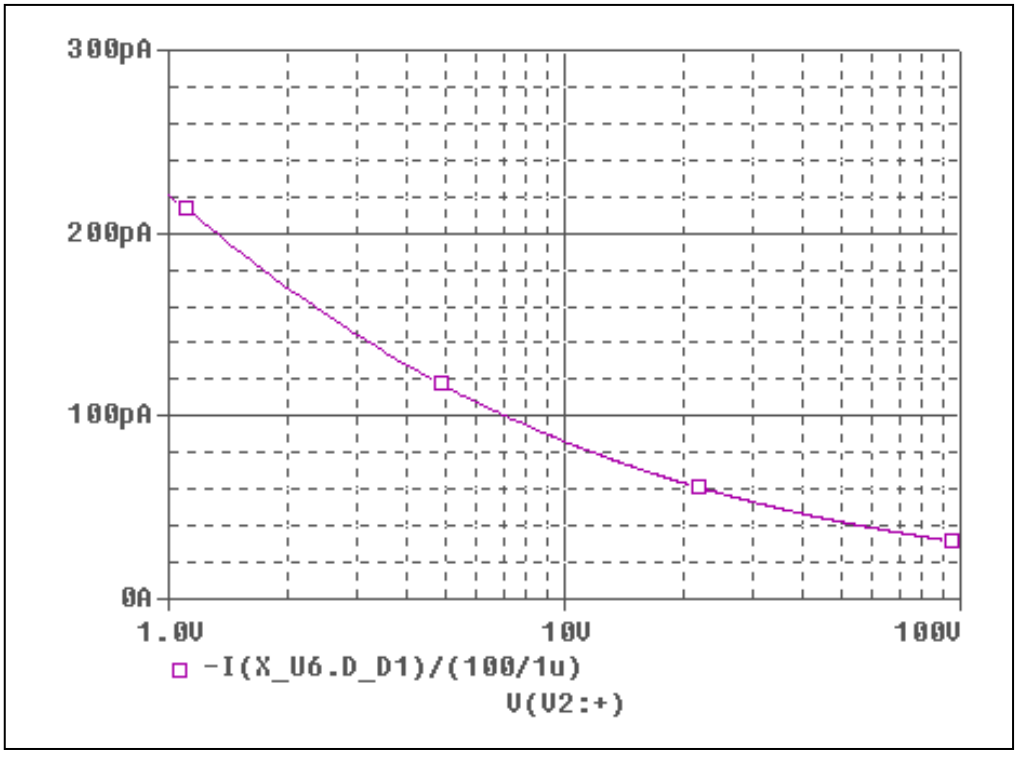


Simulation Result

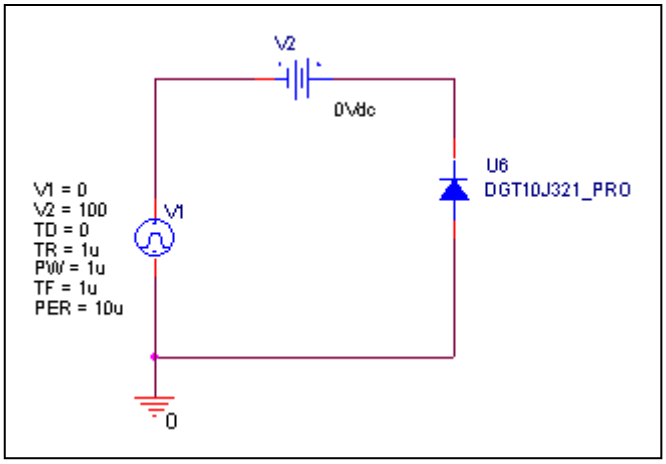
Ifwd(A)	Vfwd(V) Measurement	Vfwd(V) Simulation	%Error
0.1	0.705	0.7065	0.21277
0.2	0.77	0.7696	-0.05195
0.5	0.875	0.8764	0.16000
1	0.96	0.967	0.72917
2	1.055	1.0604	0.51185
5	1.2	1.1799	-1.67500
9	1.245	1.2591	1.13253

Junction Capacitance Characteristic

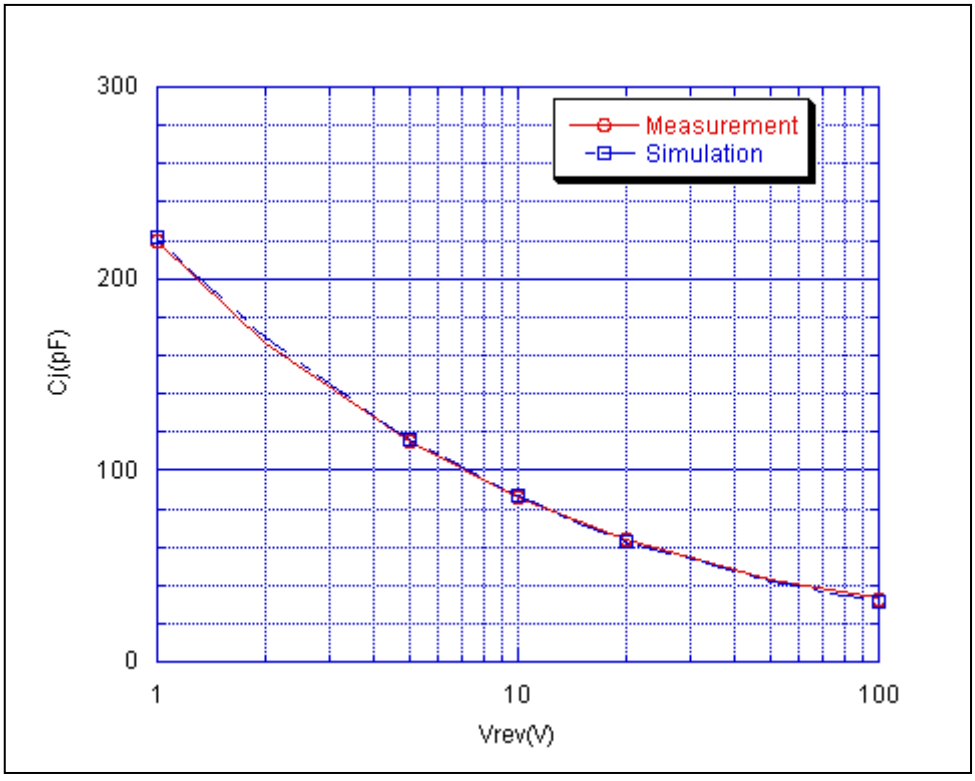
Circuit Simulation Result



Evaluation Circuit



Comparison Graph

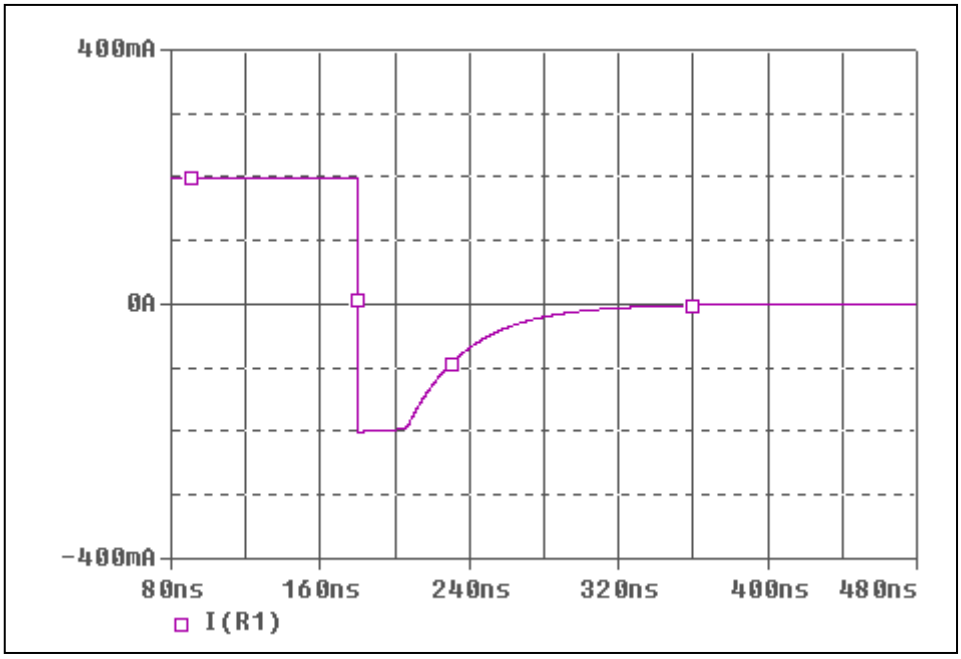


Simulation Result

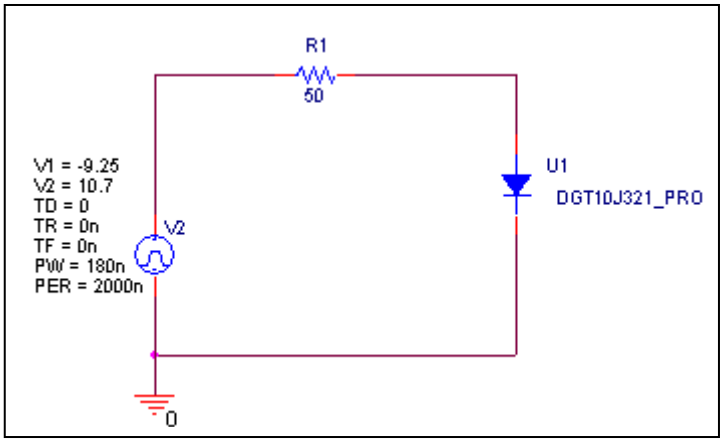
Vrev(V)	Cj(pF) Measurement	Cj(pF) Simulation	%Error
1	219.493	221.226	0.78955
2	165.947	169.489	2.13442
5	114.745	116.284	1.34123
10	85.8867	86.326	0.51149
20	63.8756	63.285	-0.92461
50	43.034	42.249	-1.82414
100	31.9336	30.902	-3.23045

Reverse Recovery Characteristic

Circuit Simulation Result



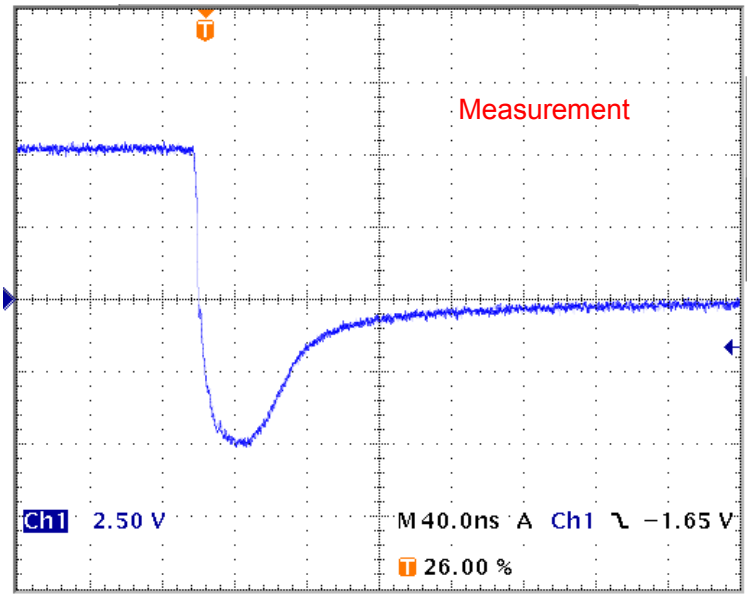
Evaluation Circuit



Compare Measurement vs. Simulation

	Measurement		Simulation		Error(%)
trj	25.6	ns	25.692	ns	0.359
trb	73.6	ns	73.310	ns	0.397

Reverse Recovery Characteristic Reference



trj=25.6(ns)

trb=73.6(ns)

Conditions:Ifwd=Irev=0.2(A),Rl=50