

Device Modeling Report

COMPONENTS: Insulated Gate Bipolar Transistor (IGBT)
PART NUMBER: GT15J101
MANUFACTURER: TOSHIBA

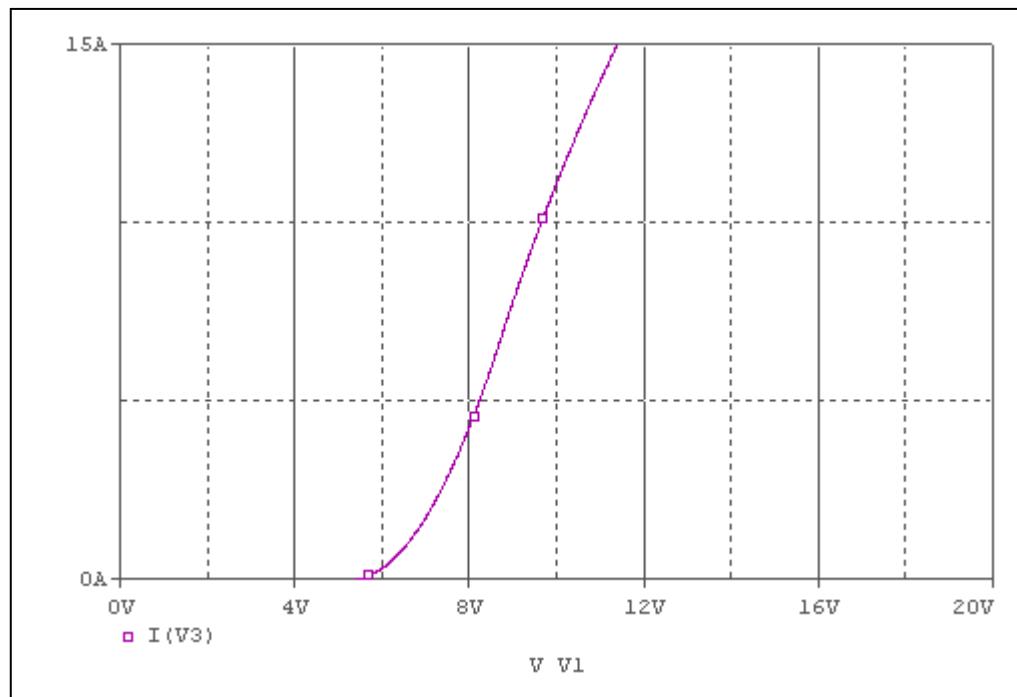


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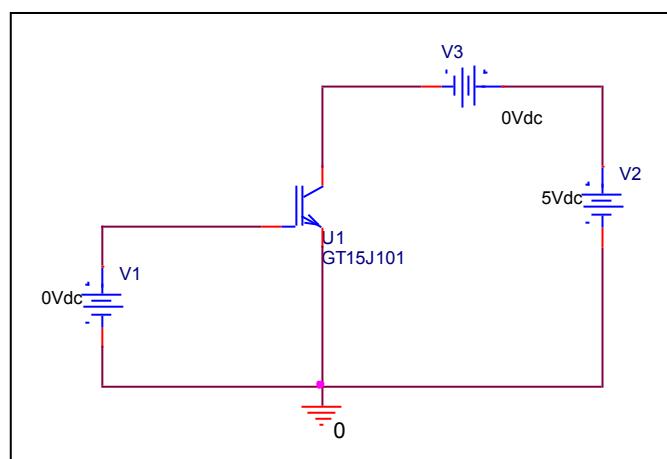
PSpice model parameter	Model description
TAU	Ambipolar Recombination Lifetime
KP	MOS Transconductance
AREA	Area of the Device
AGD	Gate-Drain Overlap Area
WB	Metallurgical Base Width
VT	Threshold Voltage
KF	Triode Region Factor
CGS	Gate-Source Capacitance per Unit Area
COXD	Gate-Drain Oxide Capacitance per Unit Area
VTD	Gate-Drain Overlap Depletion Threshold

Transfer Characteristics

Circuit Simulation result

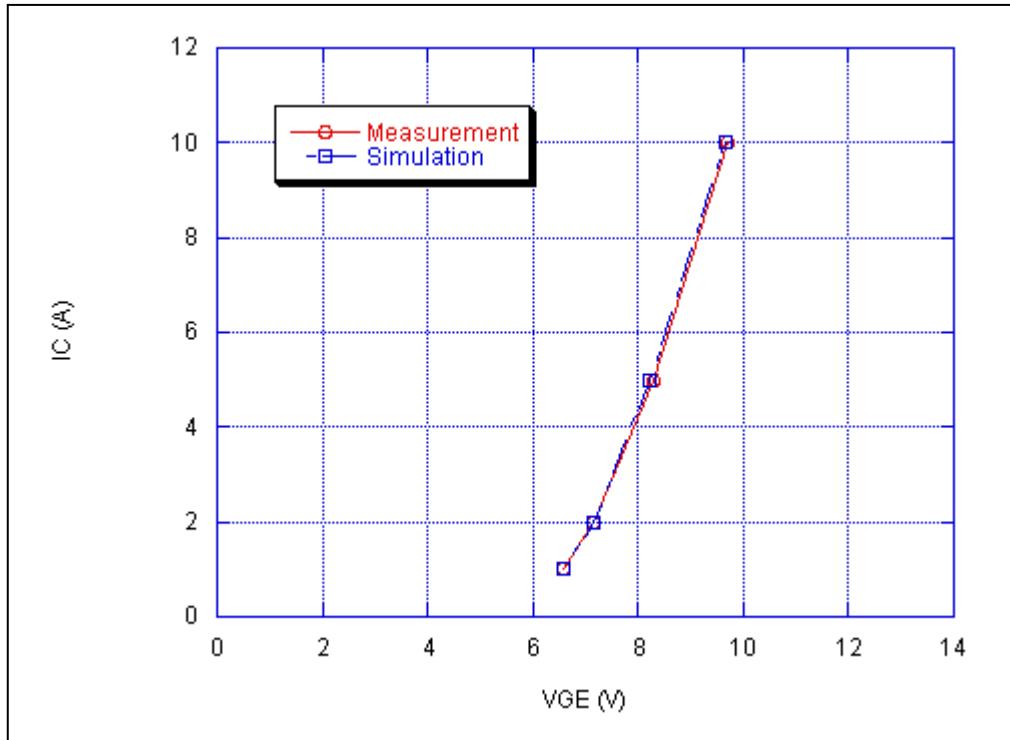


Evaluation circuit



Comparison Graph

Circuit Simulation Result



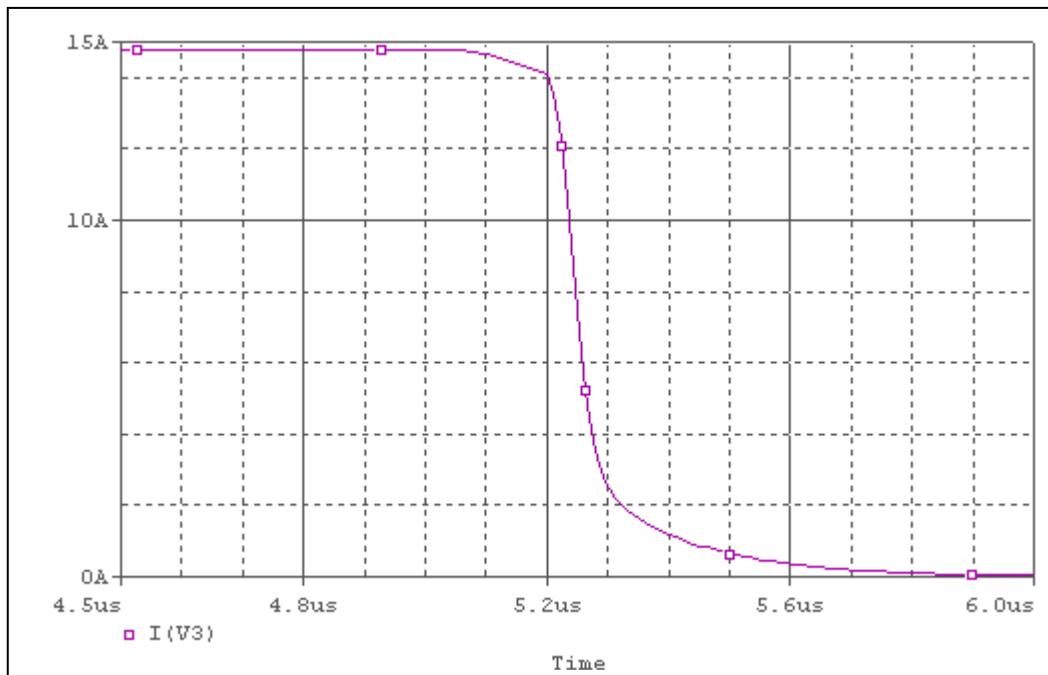
Simulation Result

Test condition : $V_{ce} = 5$ V

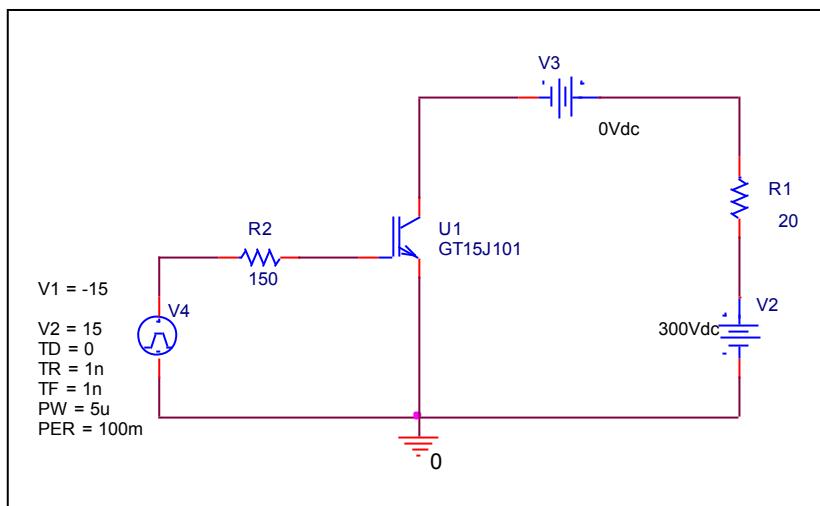
I_c (A)	V_{ge} (V)		Error (%)
	Measurement	Simulation	
1	6.6	6.6067	0.10152
2	7.15	7.1461	-0.05455
5	8.3	8.2247	-0.90723
10	9.7	9.506	-2.00000

Fall Time Characteristics

Circuit Simulation result



Evaluation circuit

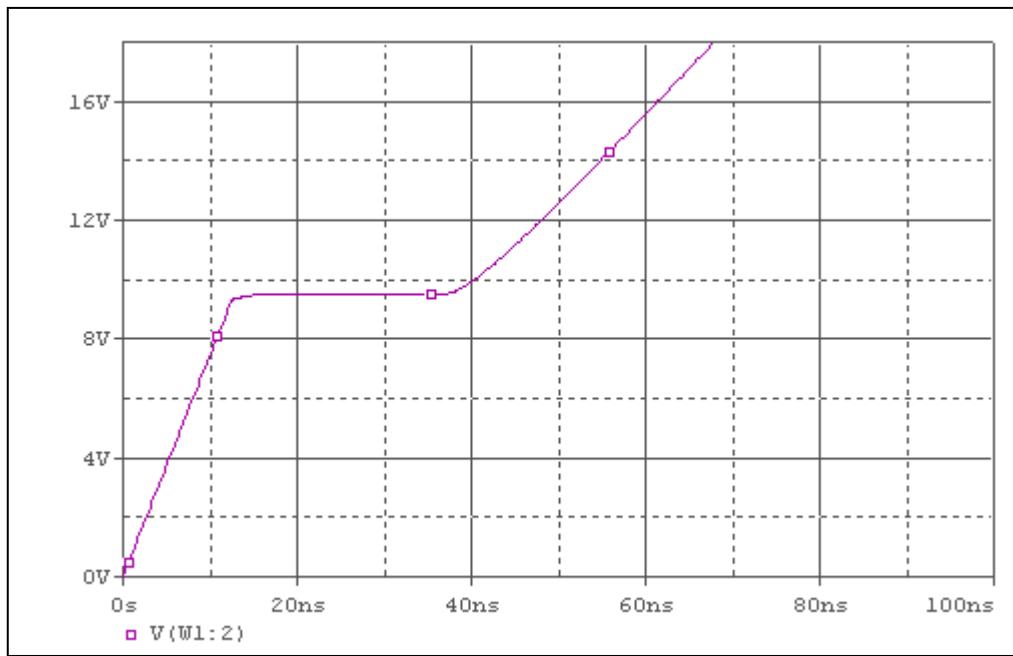


Test condition $I_c=15(A)$, $V_{ce}=300(V)$

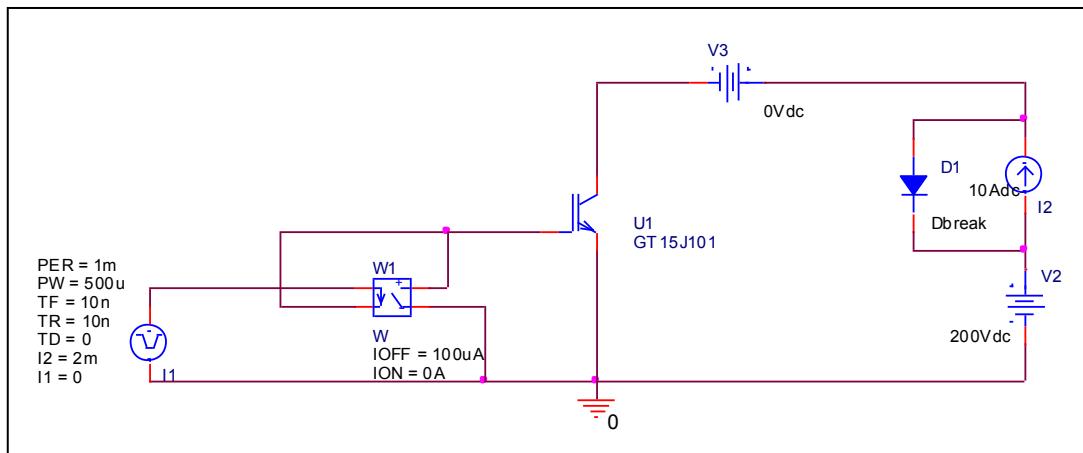
tf	Measurement		Simulation		Error
	150	ns	149.839	ns	-0.10733

Gate Charge Characteristics

Circuit Simulation result



Evaluation circuit

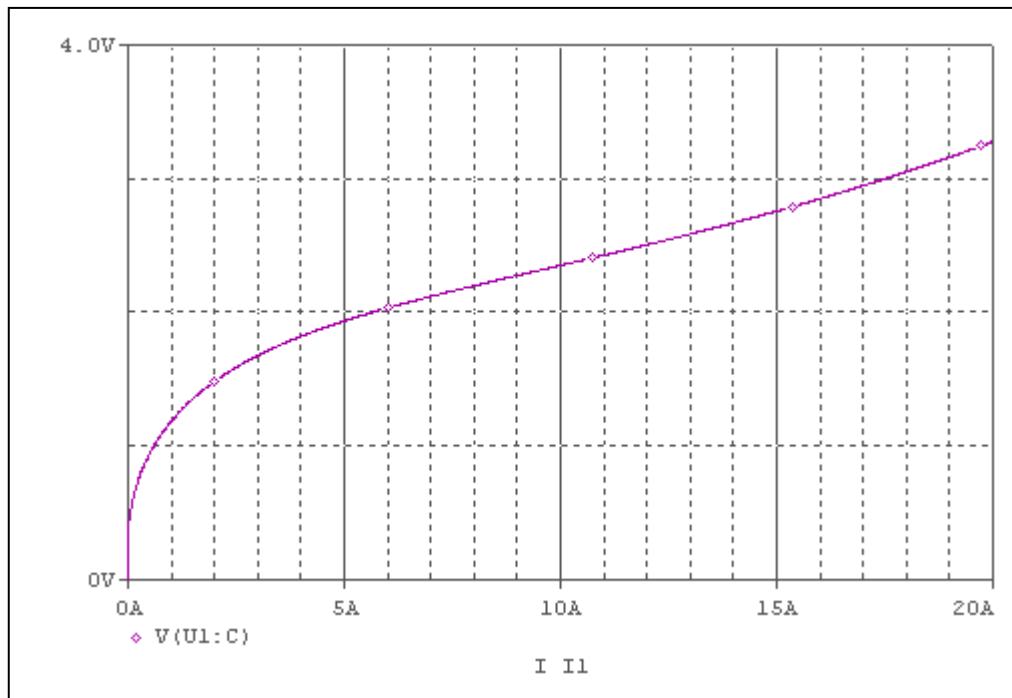


Test condition : $V_{cc}=200(V)$, $I_c=20(A)$, $V_{ge}=16(V)$

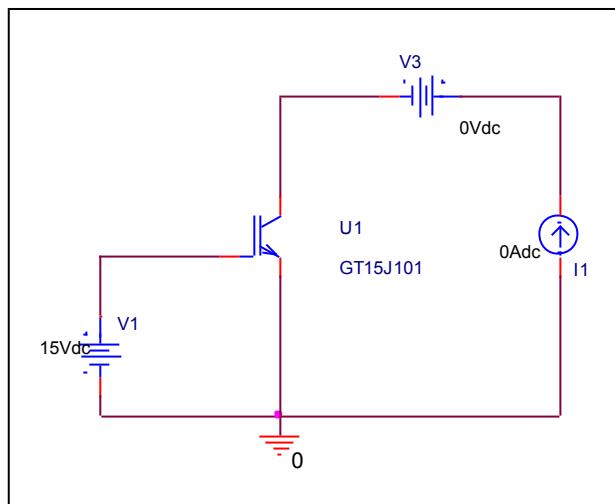
	Measurement		Simulation		Error(%)
Q_{ge}	12.5	nc	12.644	nc	1.15200
Q_{gc}	24	nc	23.908	nc	-0.38333
Q_g	61.5	nc	61.15	nc	-0.56911

Saturation Characteristics

Circuit Simulation result

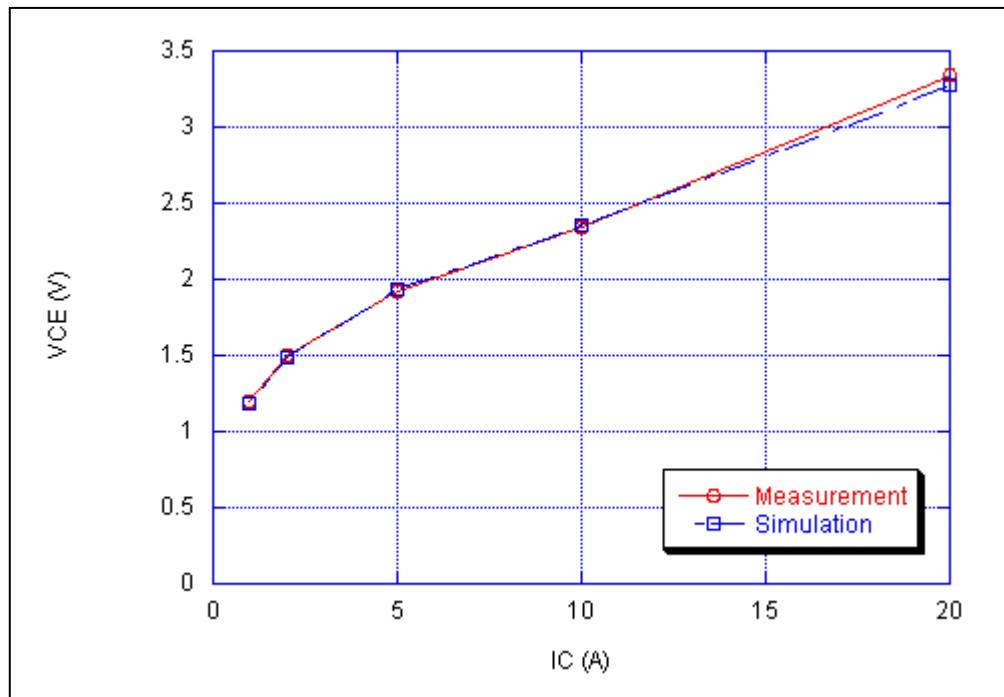


Evaluation circuit



Comparison Graph

Circuit Simulation Result



Simulation Result

Ic(A)	Vce(sat)(V)		Error (%)
	Measurement	Simulation	
1	1.2	1.1853	-1.22500
2	1.5	1.4835	-1.10000
5	1.925	1.9355	0.54545
10	2.35	2.3515	0.06383
20	3.35	3.2773	-2.17015