Device Modeling Report

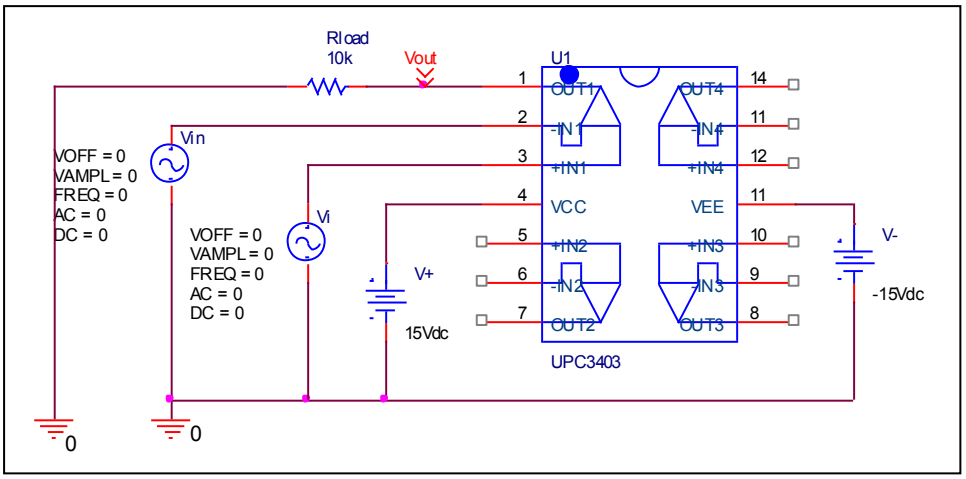
COMPONENTS:MOSFET: OPERATIONAL AMPLIFIER
PART NUMBER:uPC3403G2
MANUFACTURER:NEC ELECTRONICS

Bee Technologies Inc.

All Rights Reserved Copyright (c) Bee Technologies Inc. 2004

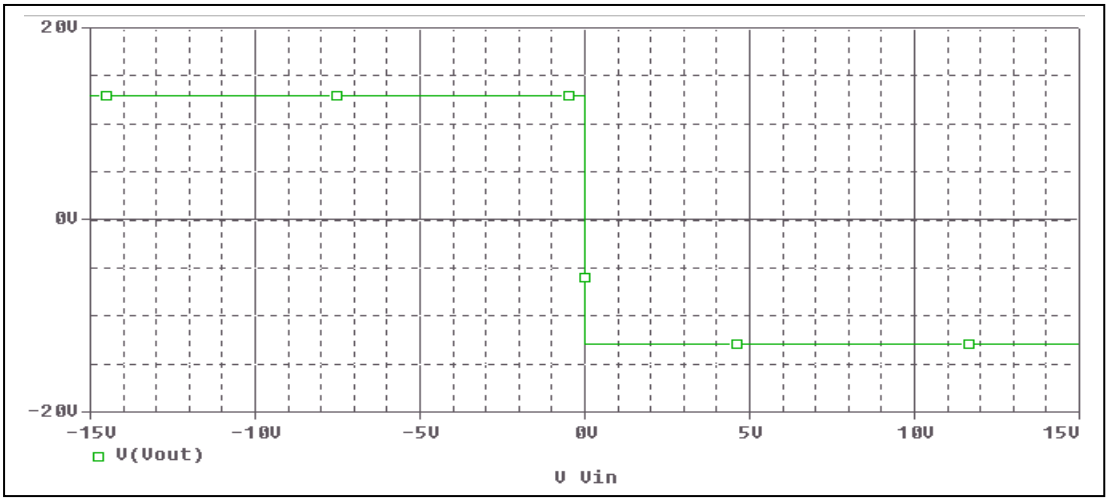
Output Voltage Swing, +Vout and –Vout

Evaluation circuit



The output voltage change of Opamp(open loop) when input DC voltage (Vin -Vi) is changed with the evaluation circuit is simulated

Simulation result



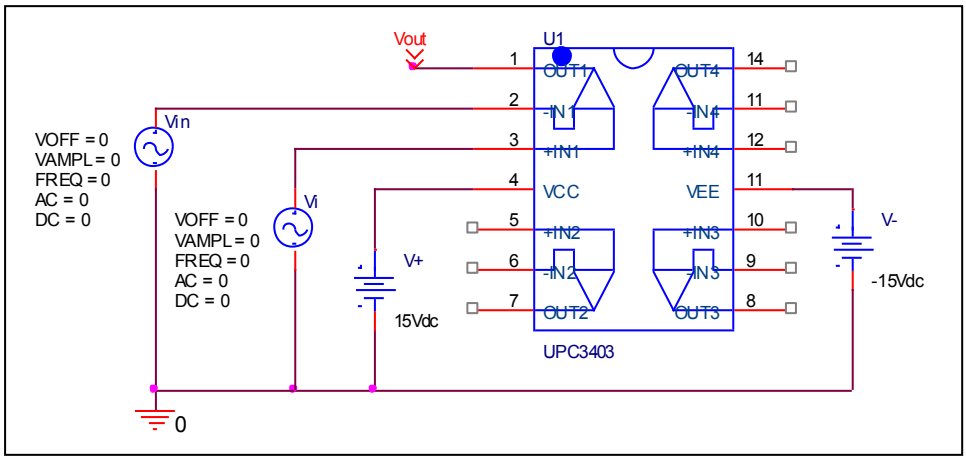
These simulation results are compared with ±Vout

Output Voltage Swing	Data sheet	Simulation	%Error
+Vout(V)	+13	+12.999	0.0076
-Vout(V)	-13	-12.999	0.0076

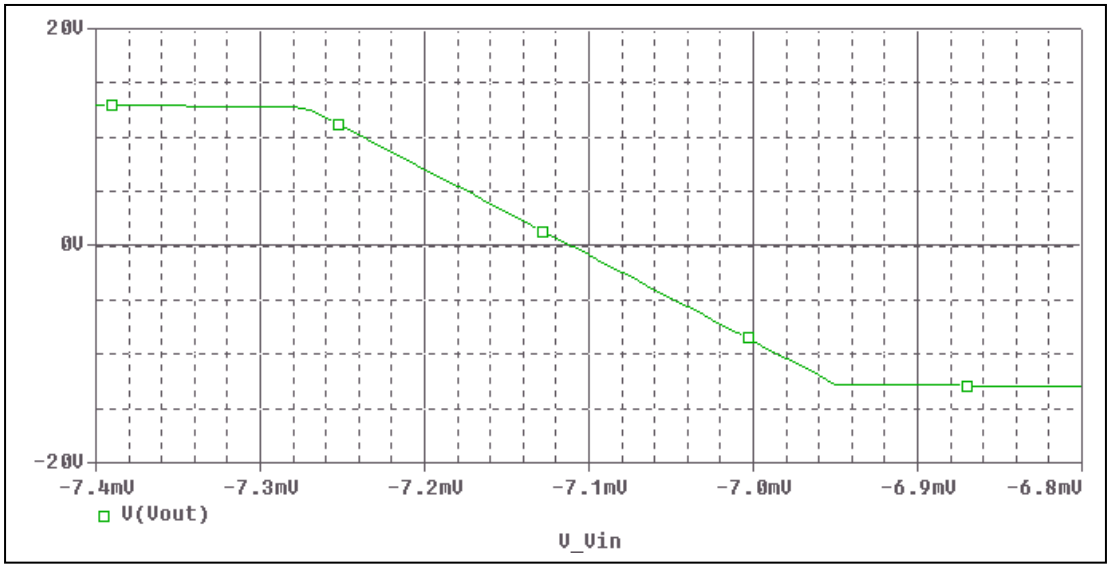
All Rights Reserved Copyright (c) Bee Technologies Inc. 2004

Input Offset Voltage

Evaluation circuit



Simulation result

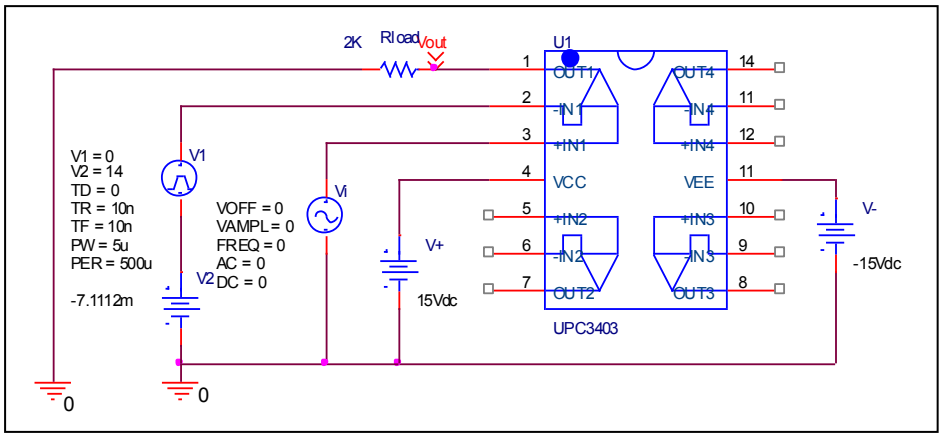


	Measurement		Simulation		Error	
Vos	7	mV	7.1112	mV	1.591	%

All Rights Reserved Copyright (c) Bee Technologies Inc. 2004

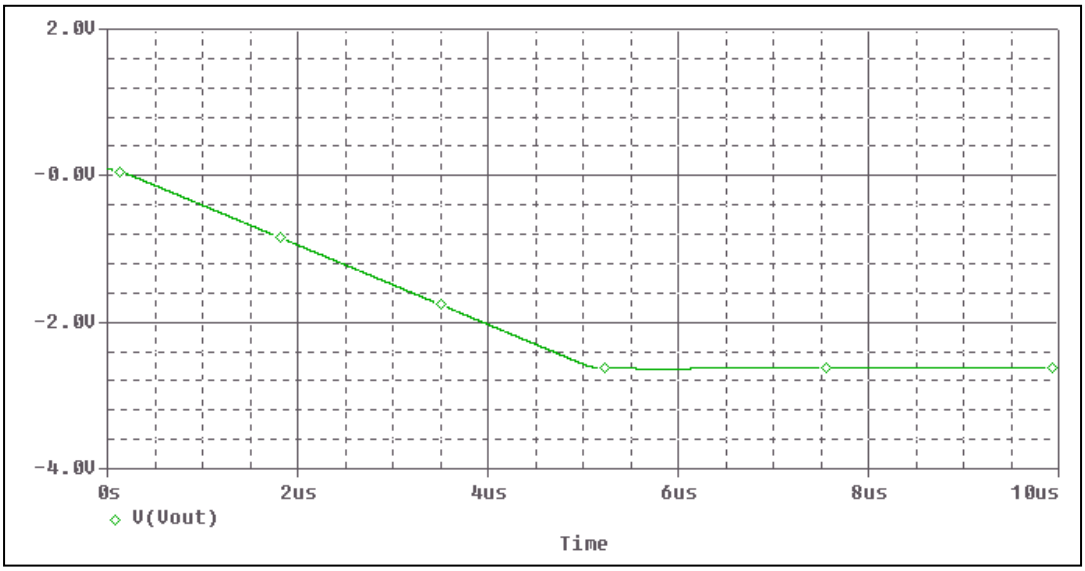
Slew Rate, +SR, -SR

Evaluation circuit



The output voltage change versus time (slope) of op-amp when input electric step voltage.

Simulation result



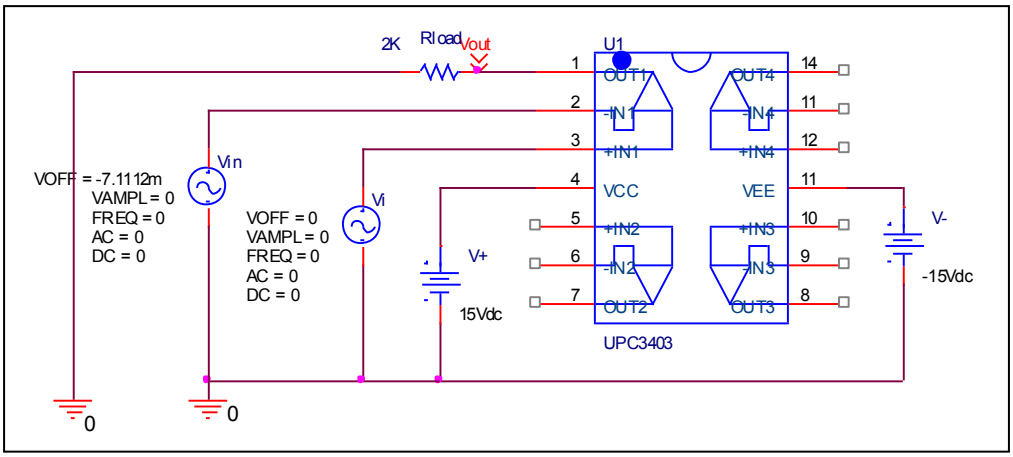
Output voltage change 0.5V in 1 us (If no good can change **C2** of Spice Model Editor)

Slew Rate(v/us)	Data sheet	Simulation	%Error
	0.5	0.491	1.8

All Rights Reserved Copyright (c) Bee Technologies Inc. 2004

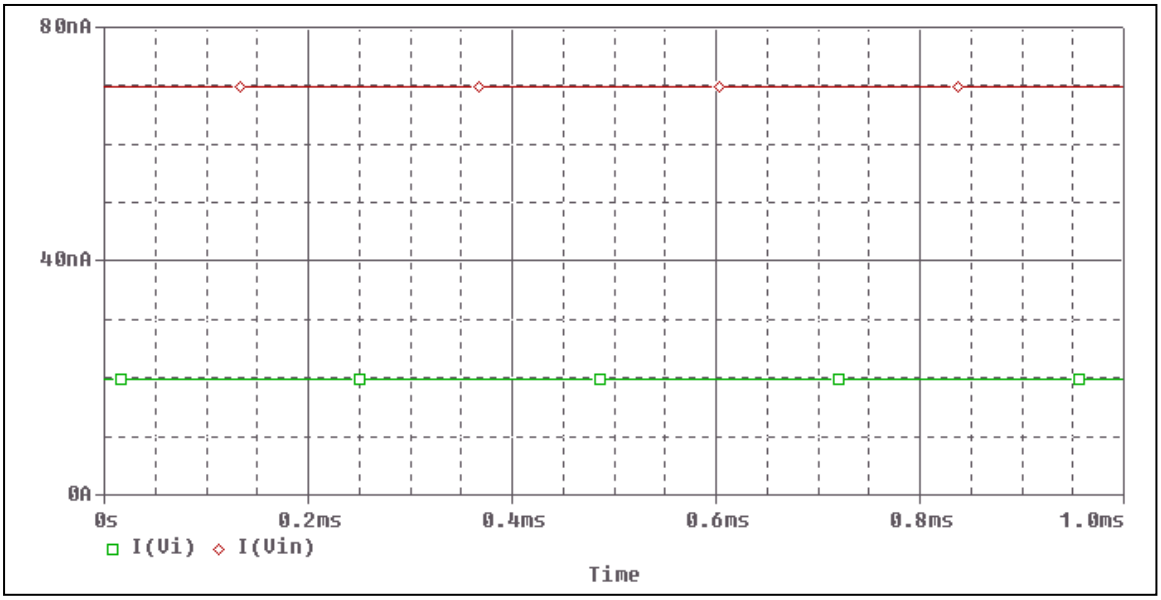
Input current Ib, Ibos

Evaluation circuit



The input offset current when supply voltage to op-amp

Simulation result

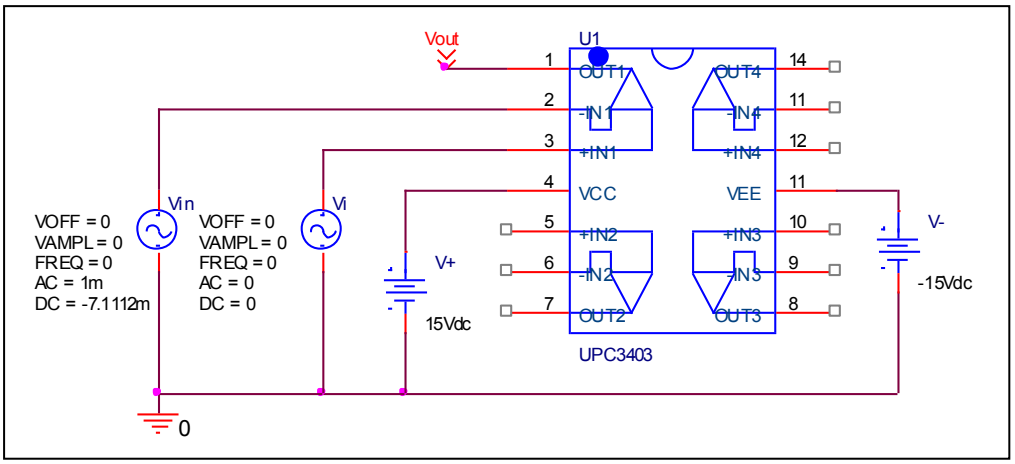


	Data sheet	Simulation	%Error
Ib(nA)	45	44.845	0.344
Ibos(nA)	50	49.87	0.26

All Rights Reserved Copyright (c) Bee Technologies Inc. 2004

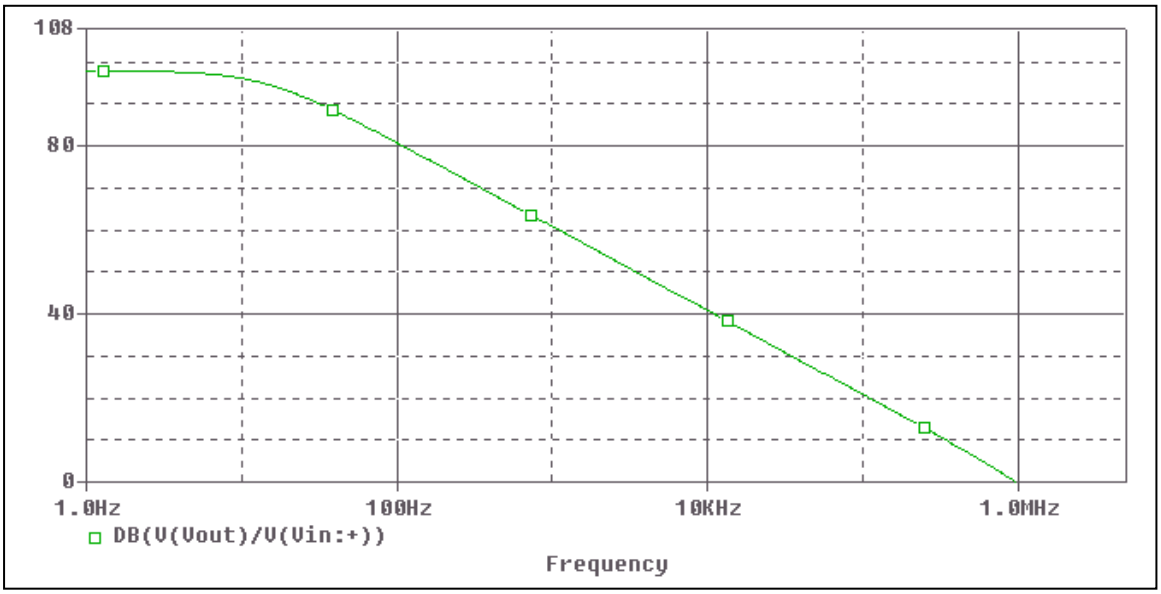
Open Loop Voltage Gain vs. Frequency , Av-dc, f-0dB

Evaluation circuit



The open loop voltage gain of op-amp when supply AC input voltage 1MHz frequecy

Simulation result

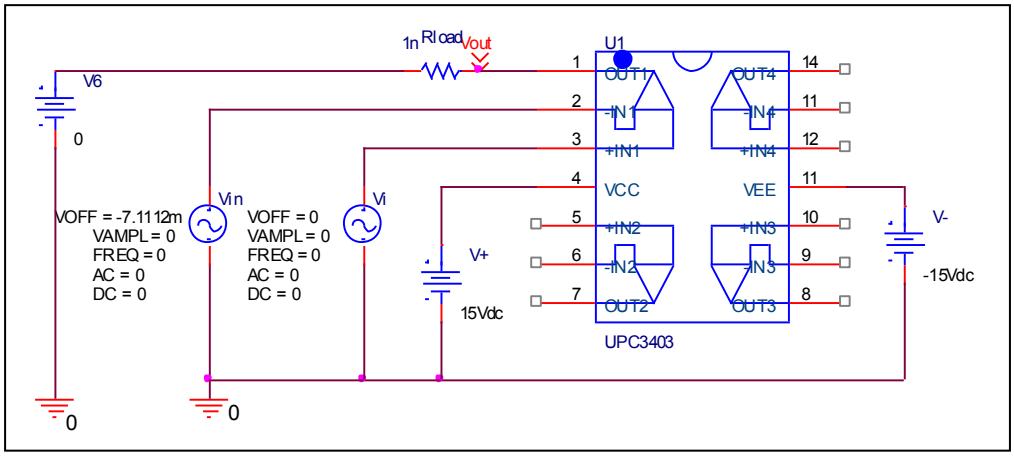


	Data sheet	Simulation	%Error
f-0dB(MHz)	1	0.985	1.5
Av-dc	79432	79031	0.504

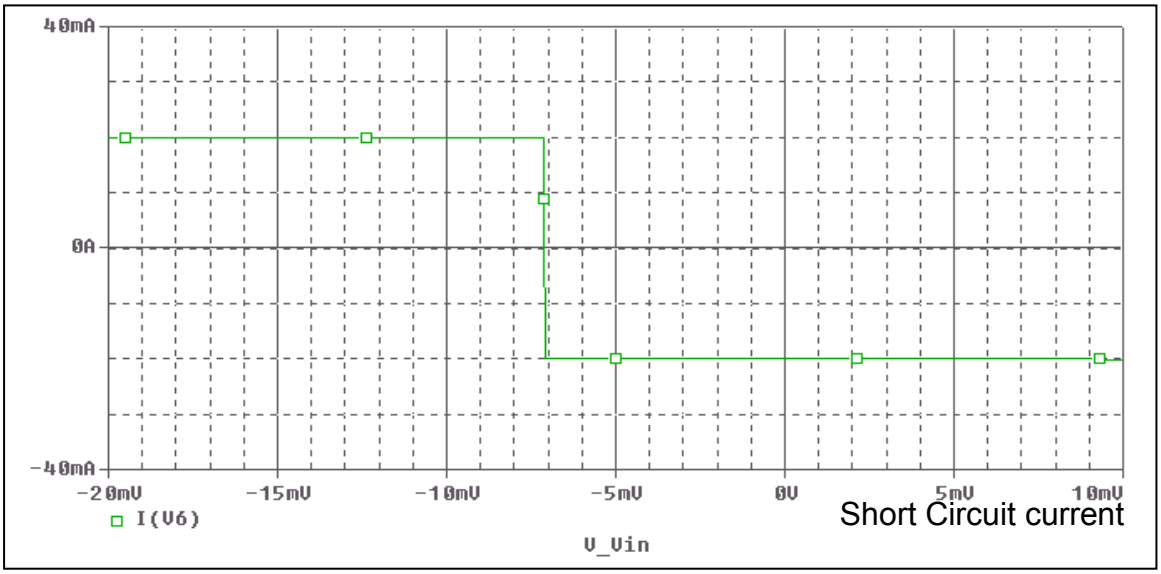
All Rights Reserved Copyright (c) Bee Technologies Inc. 2004

Output Short Circuit Current - Ios

Evaluation circuit



Simulation result

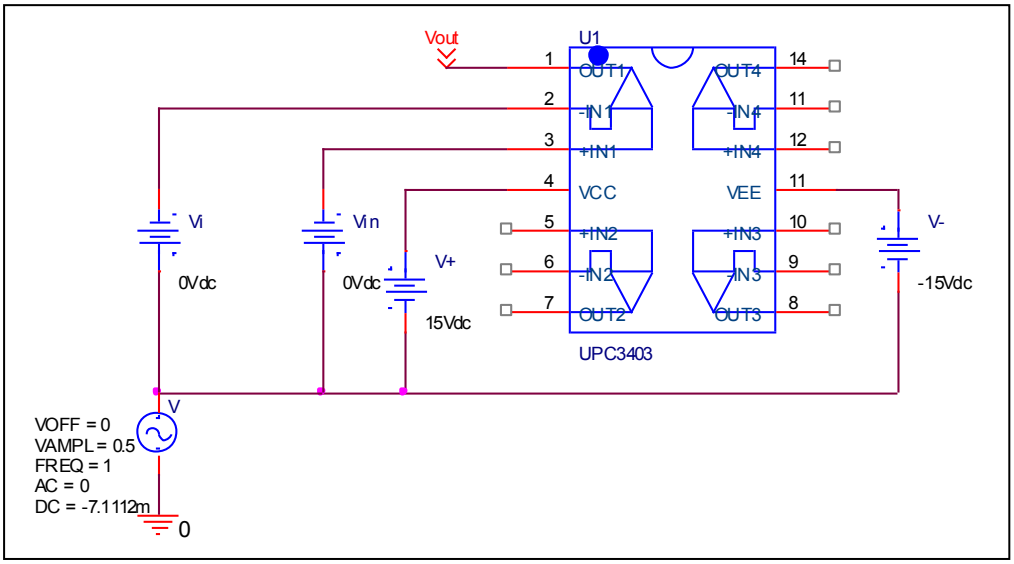


Short Circuit Current	Data sheet	Simulation	%Error
	20mA	20.064mA	0.32

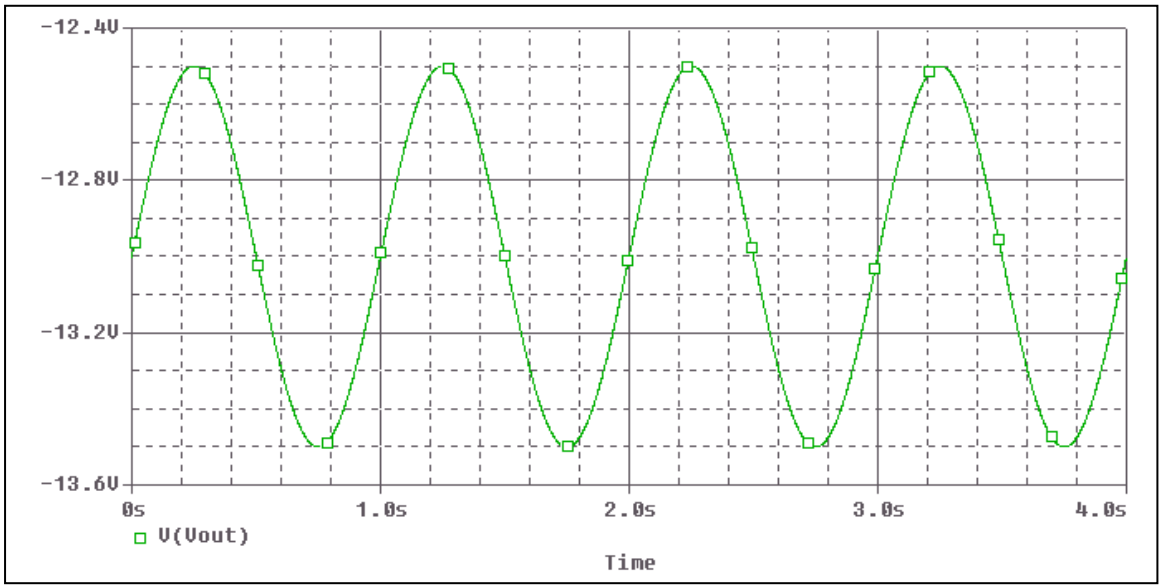
All Rights Reserved Copyright (c) Bee Technologies Inc. 2004

Common-Mode Rejection Voltage gain

Evaluation circuit



Simulation result



Common mode gain=1/0.3981
Common Mode Reject Ratio=79031/2.5519=31462

CMRR	Data sheet	Simulation	%Error
	31622	31462	0.5

All Rights Reserved Copyright (c) Bee Technologies Inc. 2004