

Device Modeling Report

COMPONENTS : OPERATIONAL AMPLIFIER (CMOS)
PART NUMBER : TC75S60FU
MANUFACTURER : TOSHIBA



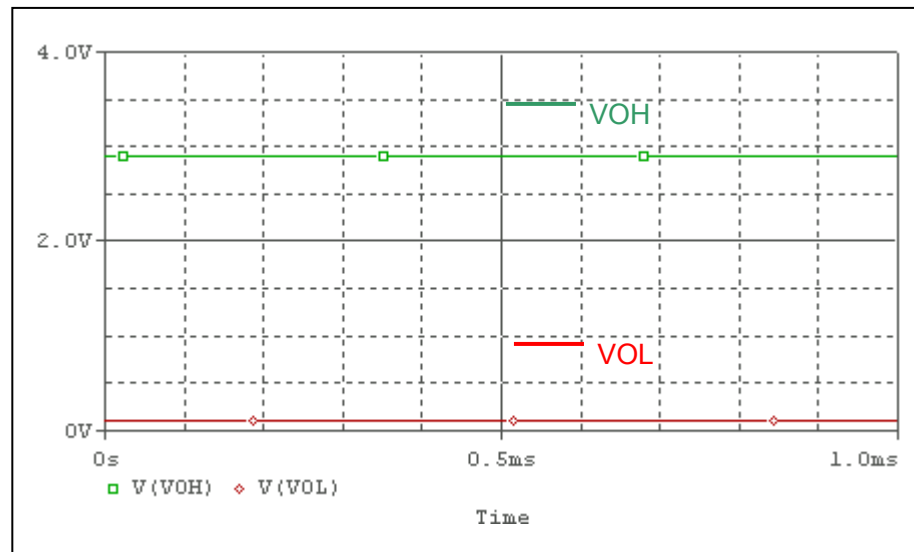
Bee Technologies Inc.

MOSFET MODEL

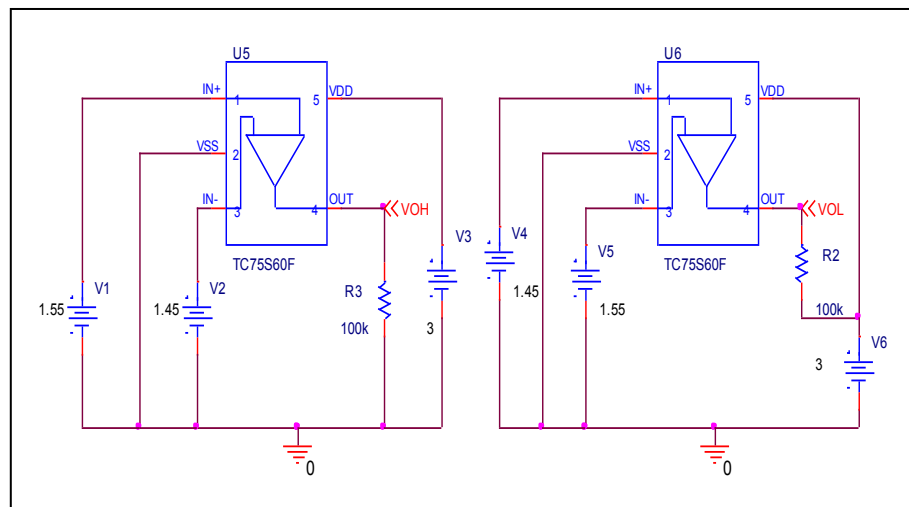
Pspice model parameter	Model description
LEVEL	
L	Channel Length
W	Channel Width
KP	Transconductance
RS	Source Ohmic Resistance
RD	Ohmic Drain Resistance
VTO	Zero-bias Threshold Voltage
RDS	Drain-Source Shunt Resistance
TOX	Gate Oxide Thickness
CGSO	Zero-bias Gate-Source Capacitance
CGDO	Zero-bias Gate-Drain Capacitance
CBD	Zero-bias Bulk-Drain Junction Capacitance
MJ	Bulk Junction Grading Coefficient
PB	Bulk Junction Potential
FC	Bulk Junction Forward-bias Capacitance Coefficient
RG	Gate Ohmic Resistance
IS	Bulk Junction Saturation Current
N	Bulk Junction Emission Coefficient
RB	Bulk Series Resistance
PHI	Surface Inversion Potential
GAMMA	Body-effect Parameter
DELTA	Width effect on Threshold Voltage
ETA	Static Feedback on Threshold Voltage
THETA	Modility Modulation
KAPPA	Saturation Field Factor
VMAX	Maximum Drift Velocity of Carriers
XJ	Metallurgical Junction Depth
UO	Surface Mobility

Output Voltage Swing

Simulation result



Evaluation Circuit

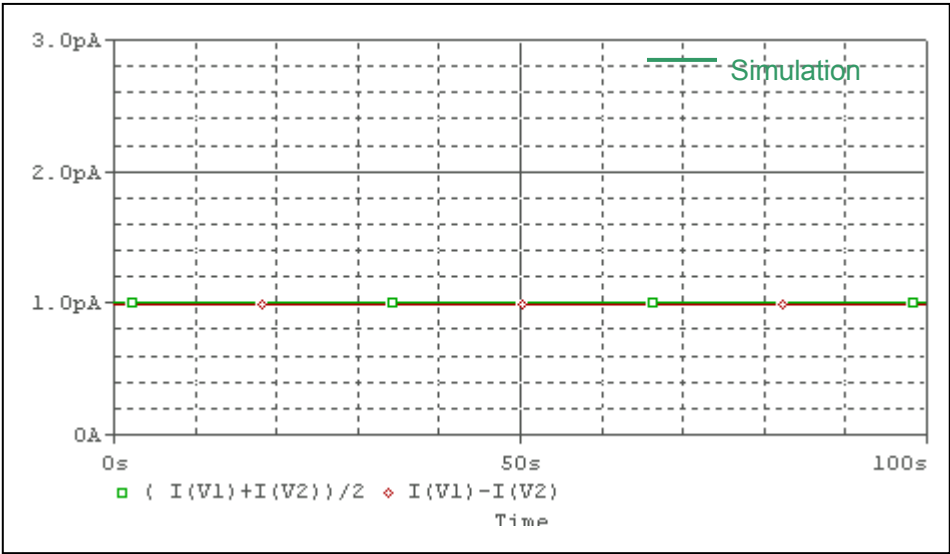


Compasion Table

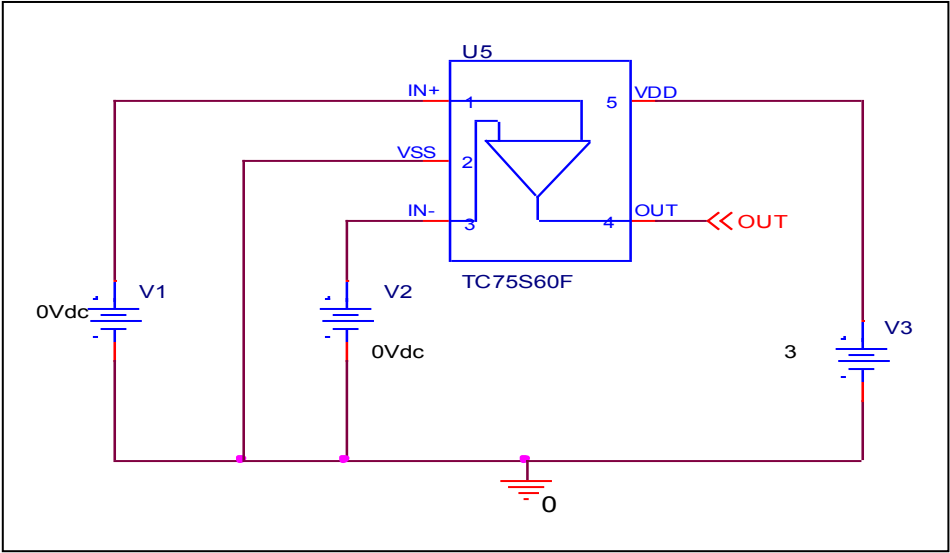
	Measurement	Simulation	%Error
$V_{OH}(V)$	2.9	2.9	0
$V_{OL}(V)$	0.1	0.1	0

Input Current

Simulation result



Evaluation Circuit

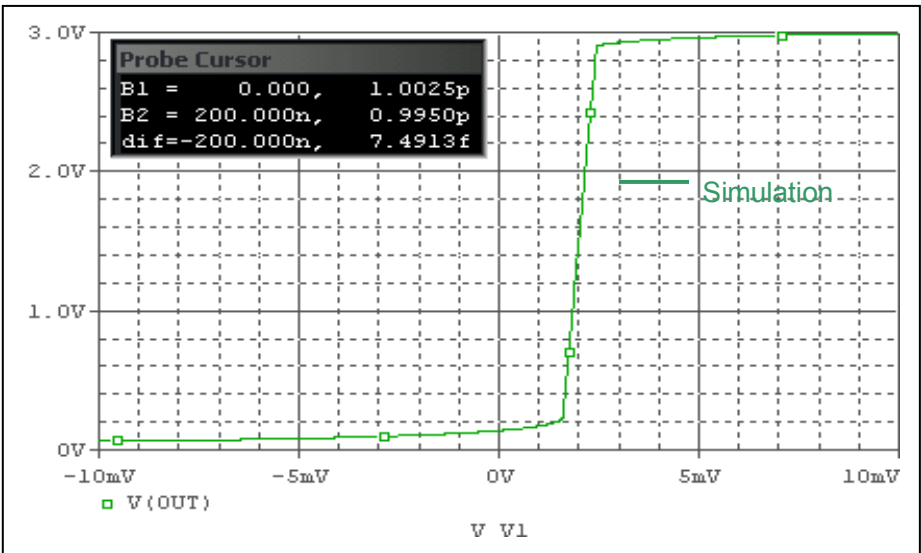


Compasion Table

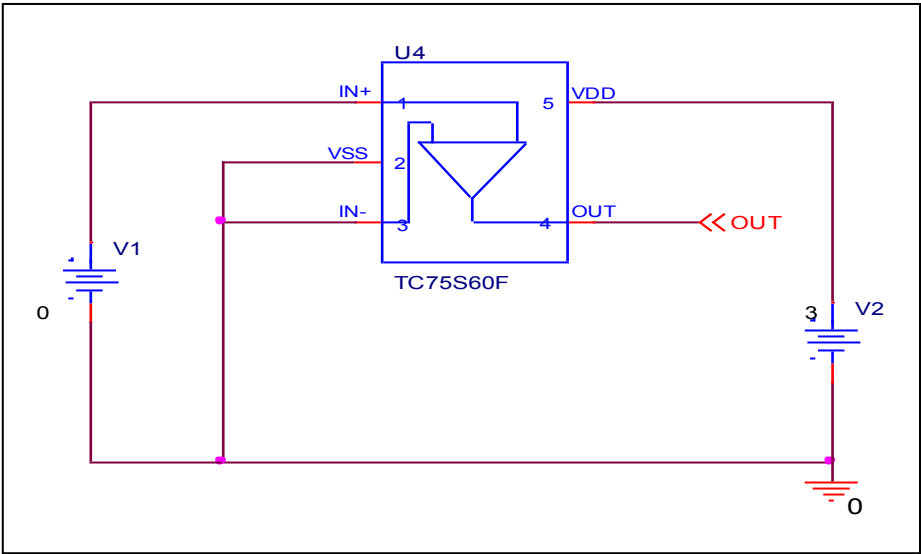
	Measurement	Simulation	% Error
I_b (pA)	1	1.002	0.2
I_{os} (pA)	1	0.995	-0.5

Input Offset Voltage

Simulation result



Evaluation Circuit

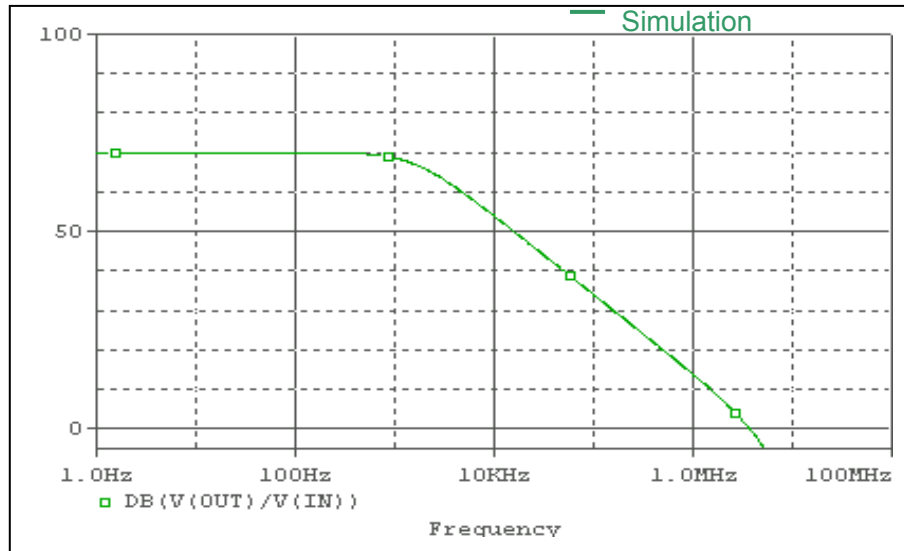


Compasion Table

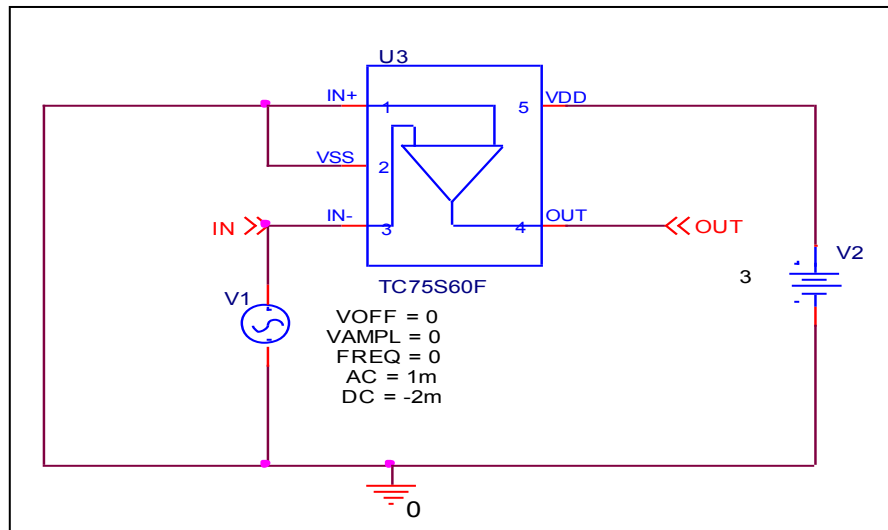
	Measurement	Simulation	%Error
V _{os} (mV)	2	2	0

Open loop Voltage Gain

Simulation result



Evaluation Circuit

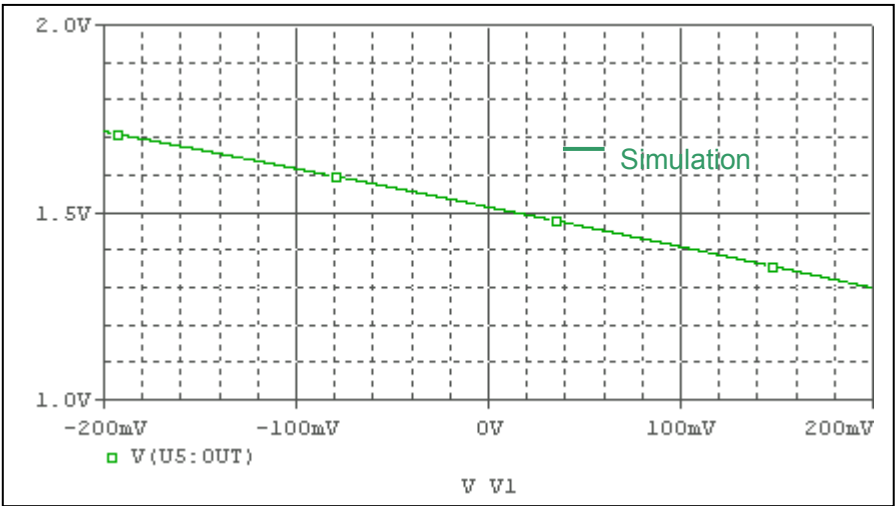


Compasion Table

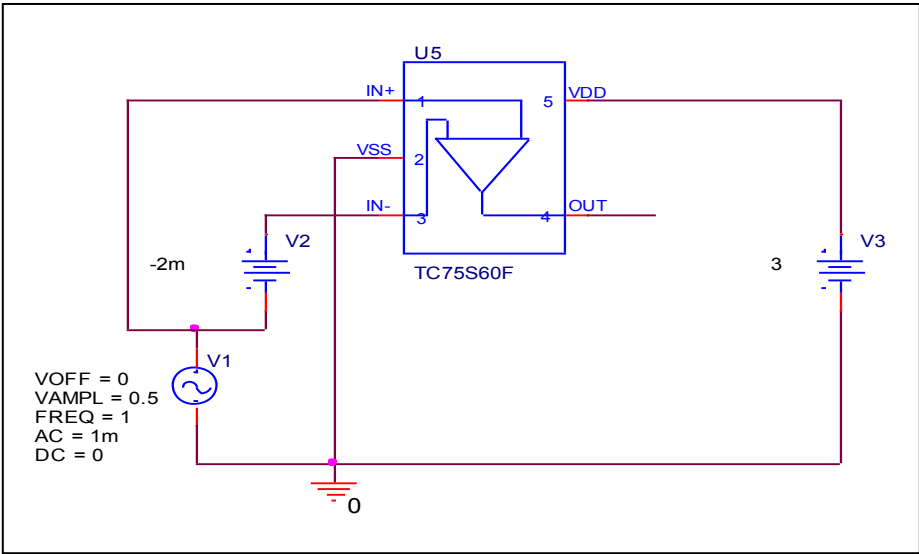
	Measurement	Simulation	%Error
Av (dB)	70	70.076	0.108
Frequency(Mhz)	3.7	3.69	-0.27

Common-Mode Rejection Ratio

Simulation result



Evaluation Circuit



$$CMRR = AV/ACM$$

Compasion Table

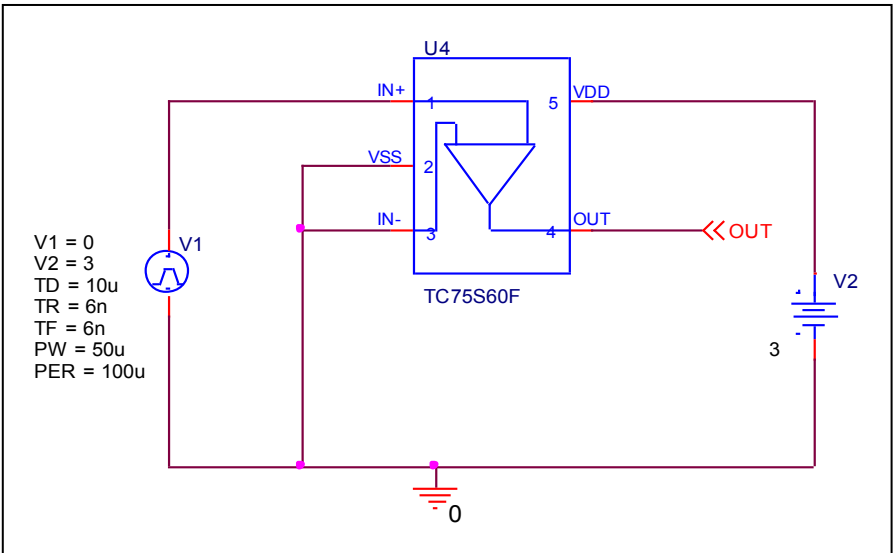
	Measurement	Simulation	%Error
CMRR (dB)	70	69.716	-0.405

Slew Rate

Simulation result



Evaluation Circuit



	Measurement	Simulation	% Error
SR (V/us)	5.1	5	-2