Device Modeling Report

COMPONENTS:SIDAC
PART NUMBER:K1V(A)14
MANUFACTURER:SHINDENGEN MFG.CO.,LTD.

Bee Technologies Inc.

SPICE MODEL

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.SUBCKT k1va14 MT2 MT1 PARAMS:
+ Vdrm=300v        Idrm=0.045E-6
+ Ih=50mA          dVdt=20e6
+ Igt=5ma          Vgt=1.5v
+ Vtm=1.6v         Itm=1A
+ Ton=1.5u
Striac    MT2      MT20     cntrol   0        Vswitch
Dak1      MT20     MT22     Dak      OFF
Vlak      MT22     MT1
Striacr   MT2      MT23     cntrolr  0        Vswitch
Dka1      MT21     MT23     Dak      OFF
Vlka      MT1      MT21
Emon      dvdt0    0        TABLE {ABS(V(MT2,MT1))} (0 0) (2000 2000)
CdVdt     dvdt0    dvdt1    100pfd
Rdlay     dvdt1    dvdt2    1k
VdVdt     dvdt2    MT1      DC 0.0
EdVdt     condvdt 0         TABLE {i(vdVdt)-100p*dVdt}   (0 0 ) (.1m 10)
RdVdt     condvdt 0         1meg
Rseries   gate     gate1    {(Vgt-0.65)/Igt}
Rshunt    gate1    gate2    {0.65/Igt}
Dgkf      gate1    gate2    Dgk
Dgkr      gate2    gate1    Dgk
Vlgf      gate2    MT1      DC 0.0
Egate     congate 0         TABLE {(ABS(i(Vlgf))-0.95*Igt)} (0 0) (1m 10)
Rgate     congate 0         1meg
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Emain1     main1     0          TABLE {i(Vlak)-Ih+5e-3*i(Vlgf)/Igt} (0 0) (.1m 1)
Rmain1     main1     0          1meg
Emain2     main2     0          TABLE {v(MT2,MT1)-(Ih*Vtm/Itm)} (0 0) (.1m 1)
Rmain2     main2     0          1meg
Emain3     cnhold    0          TABLE {v(main1,0)*v(main2,0)} (0 0 (1 10)
Rmain3     cnhold    0          1meg
Emain1r    main1r    0          TABLE {i(Vlka)-Ih-5e-3*i(Vlgf)/Igt} (0 0) (.1m 1)
Rmain1r    main1r    0          1meg
Emain2r    main2r    0          TABLE {v(MT1,MT2)-(Ih*Vtm/Itm)} (0 0) (.1m 1)
Rmain2r    main2r    0          1meg
Emain3r    cnholdr   0          TABLE {v(main1r,0)*v(main2r,0)} (0 0 (1 10)
Rmain3r    cnholdr   0          1meg
Emain4     main4     0          table {(1.0-ABS(i(Vlgf))/Igt)} (0 0) (1 1)
Rmain4     main4     0          1meg
Emain5     cnmain    0          table {v(mt2,mt1)-1.05*Vdrm*v(main4)} (0 0) (1 10)
Rmain5     cnmain    0          1meg
Emain5r    cnmainr   0          table {v(mt1,mt2)-1.05*Vdrm*v(main4)} (0 0) (1 10)
Rmain5r    cnmainr   0          1meg
Eonoff     contot    0          TABLE
+          {v(cnmain)+v(congate)+v(cnhold)+v(condvdt)} (0 0) (10 10)
Rton       contot    dlay1      825
Dton       dlay1     cntrol     Delay
Rtoff      contot    dlay2      {2.9E-3/Ton}
Dtoff      cntrol    dlay2      Delay
Cton       cntrol    0          {Ton/454}
Eonoffr    contotr   0          TABLE
+          {v(cnmainr)+v(congate)+v(cnholdr)+v(condvdt)} (0 0) (10 10)
Rtonr      contotr   dlayr1     825
Dtonr      dlayr1    cntrolr    Delay
Rtoffr     contotr   dlayr2     {2.9E-3/Ton}
Dtoffr     cntrolr   dlayr2     Delay
Ctonr      cntrolr   0          {Ton/454}
D100       10 MT2 Dvbo
D200       10 gate Dvbo
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.MODEL Vswitch vswitch
+ (Ron = {(Vtm-0.7)/Itm}, Roff = {1.75E-3*Vdrm/Idrm},
+    Von = 5.0,                    Voff = 1.5)
.MODEL    Dgk        D              (Is=1E-16 Cjo=50pf Rs=5)
.MODEL    Delay      D              (Is=1E-12 Cjo=5pf    Rs=0.01)
.MODEL    Dak        D              (Is=4E-11 Cjo=5pf)
.MODEL    Dvbo       D              (BV=140 IBV=0.2m)
Rfloat    gate       MT1 1e10
.ENDS
*$
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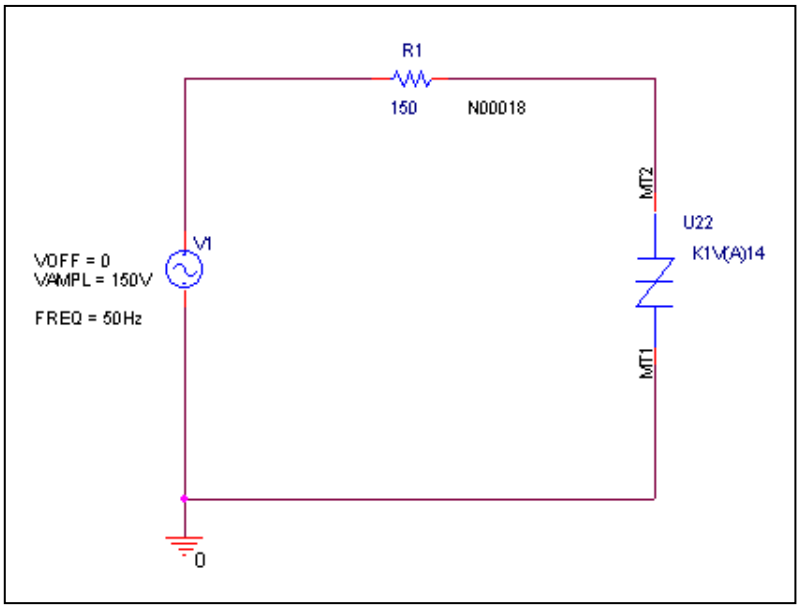
I-V Characteristic

Circuit Simulation



Simulation Result