Device Modeling Report

COMPONENTS : CMOS DIGITAL INTEGRATED CIRCUIT
PART NUMBER : TC74ACT245FT
MANUFACTURER : TOSHIBA

Bee Technologies Inc.

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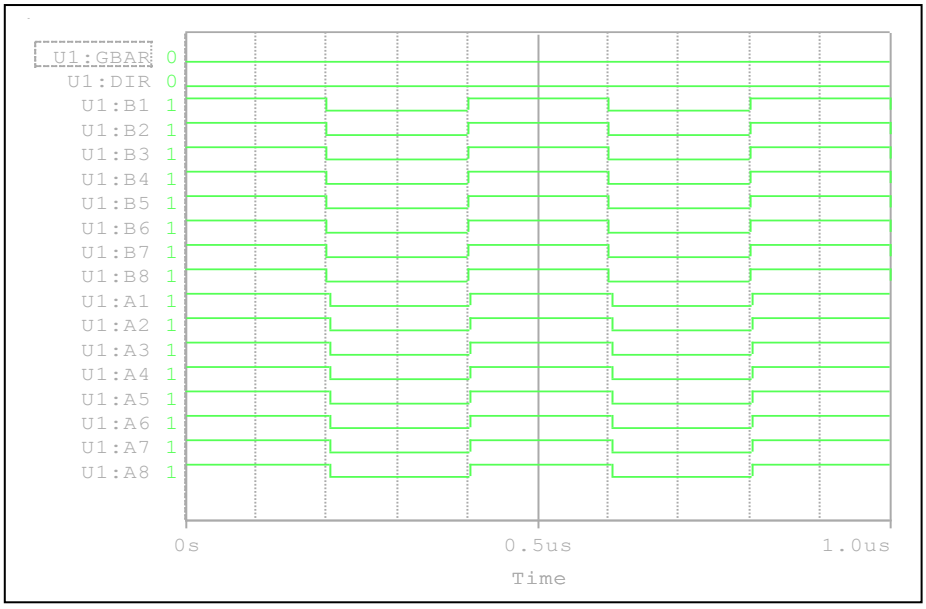
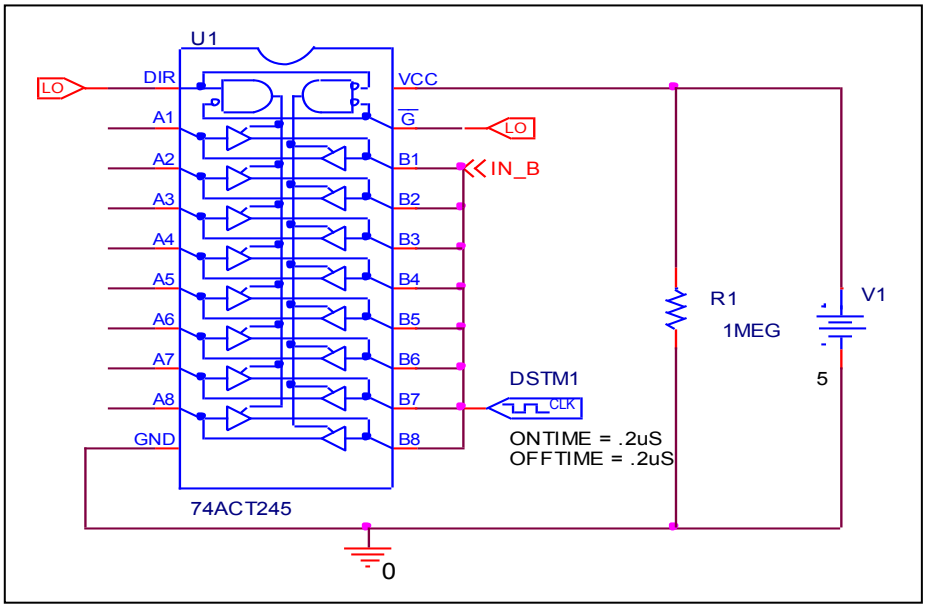
Truth Table

Circuit simulation result



Evaluation circuit



Comparison table **Function : A BUS = OUTPUT, B BUS = INPUT**

Input		Output		%Error
$\overline{G}$	DIR	Measurement	Simulation	
L	L	A=B	A=B	0

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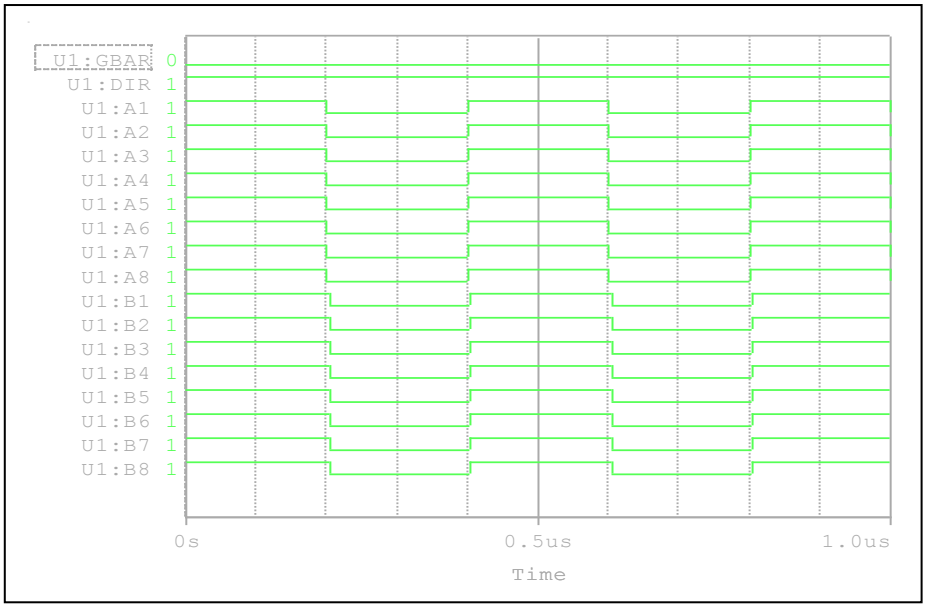
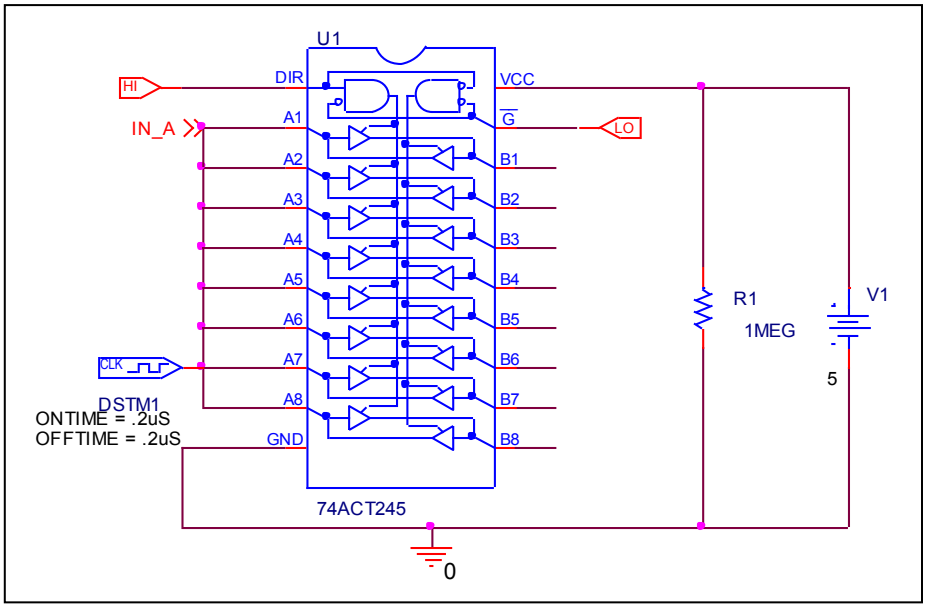
Truth Table

Circuit simulation result



Evaluation circuit



Comparison table **Function : A BUS = INPUT, B BUS = OUTPUT**

Input		Output		%Error
$\overline{G}$	DIR	Measurement	Simulation	
L	H	B=A	B=A	0

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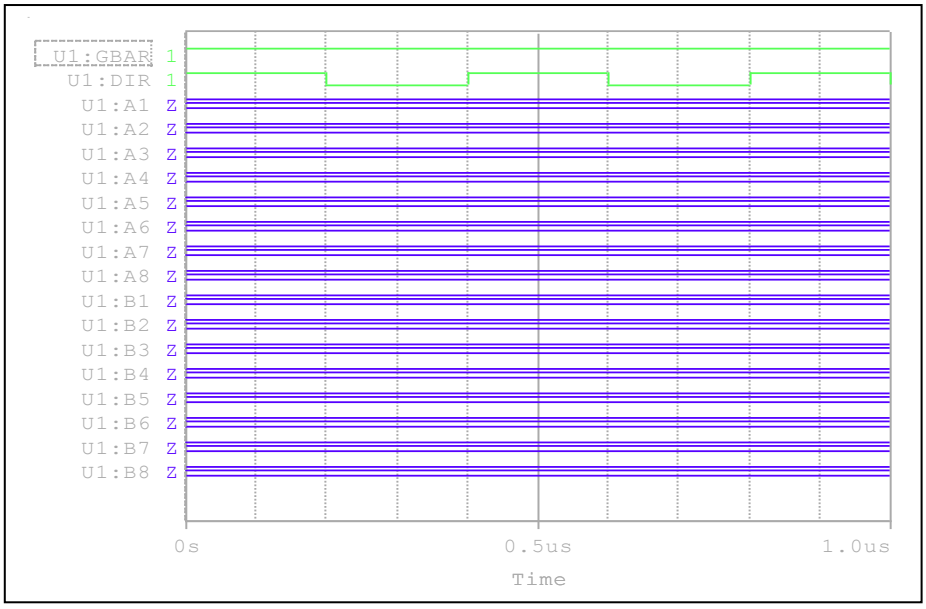
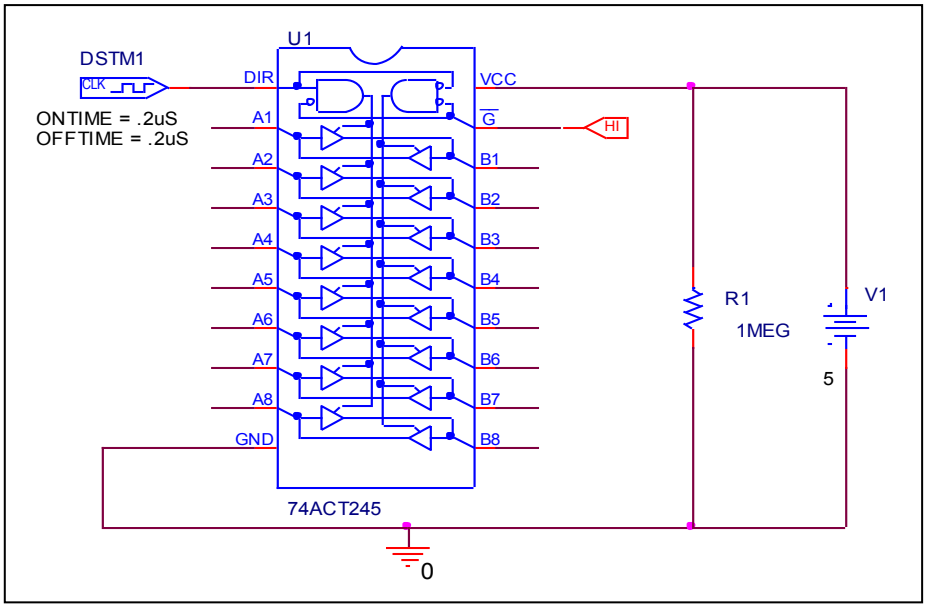
Truth Table

Circuit simulation result



Evaluation circuit



Comparison table **Function : A BUS and B BUS = HIGH IMPEDANCE**

Input		Output		%Error
$\overline{G}$	DIR	Measurement	Simulation	
H	X	Z	Z	0

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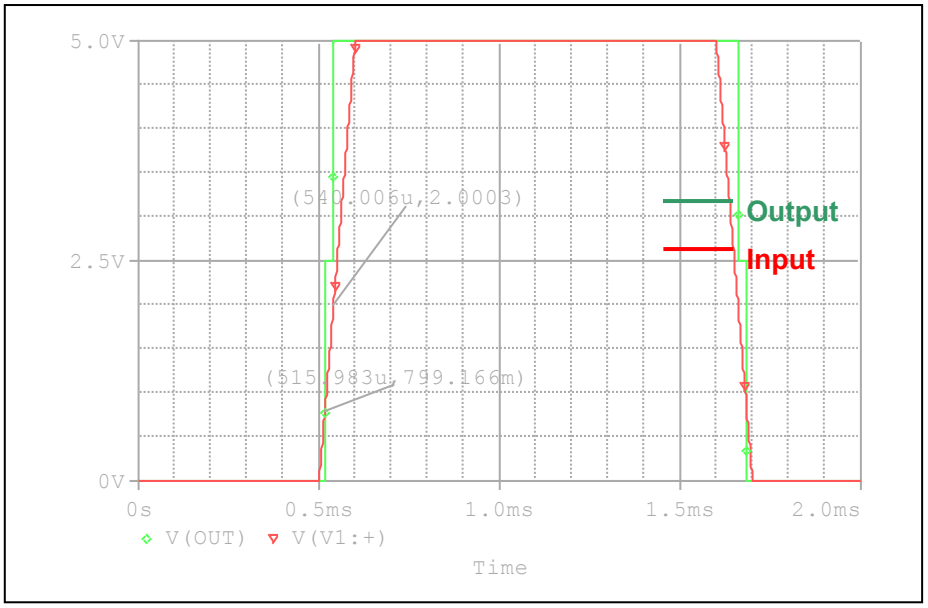
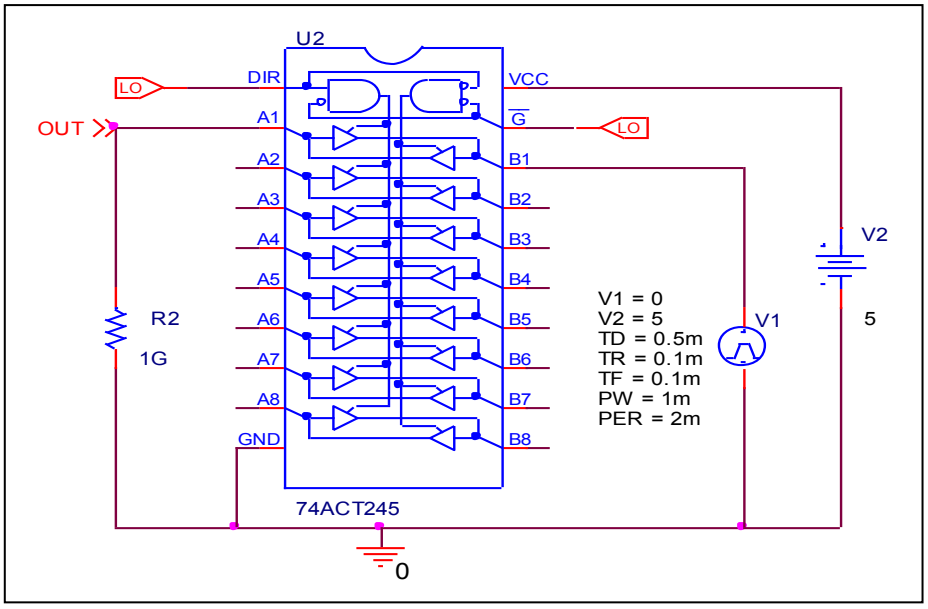
High Level and Low Level Input Voltage

Circuit simulation result



Evaluation circuit



Comparison table

V_{CC} = 5V	Measurement	Simulation	%Error
V_{IH} (V)	2	2	0
V_{IL} (V)	0.8	0.799166	-0.104

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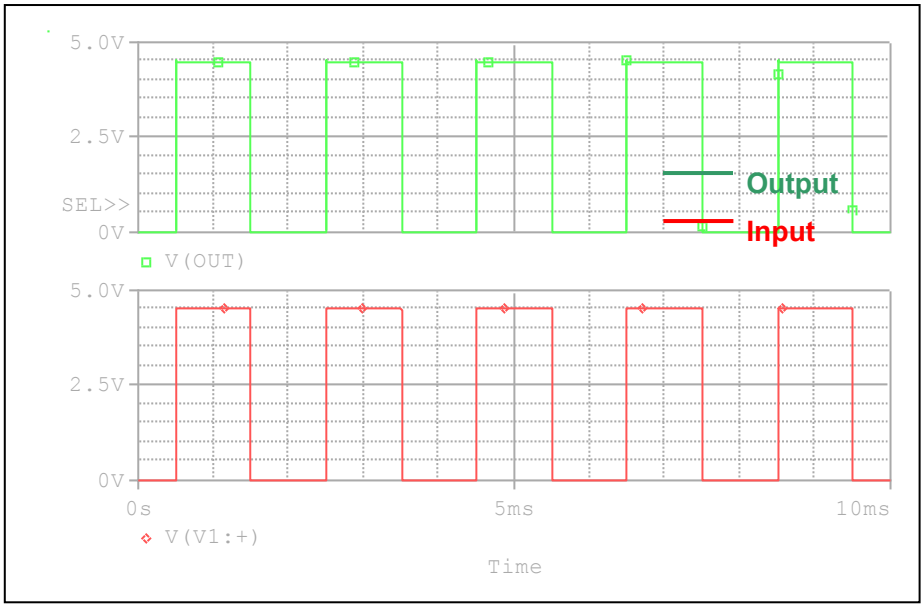
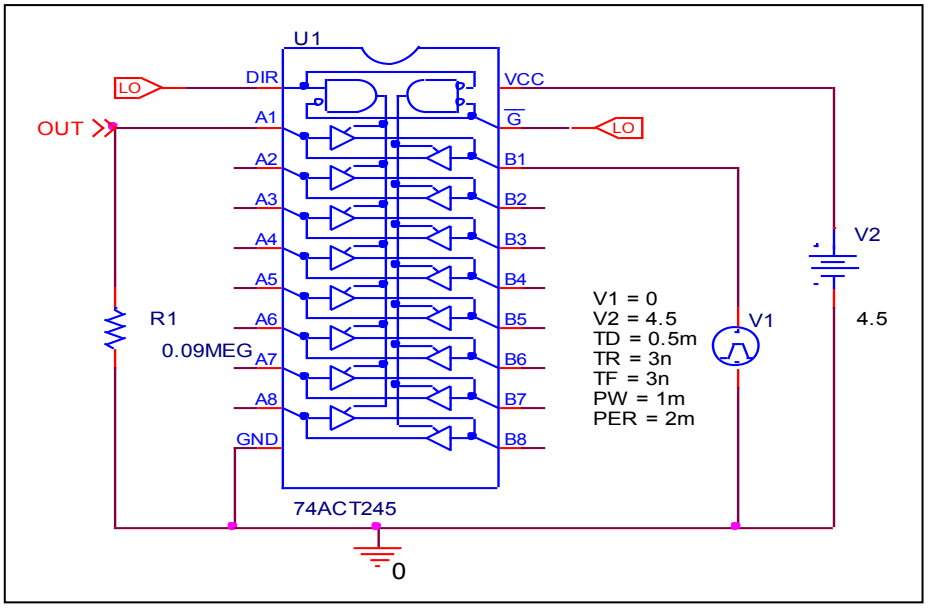
High Level and Low Level Output Voltage

Circuit simulation result



Evaluation circuit



Comparison table

V_{CC} = 4.5V	Measurement	Simulation	%Error
V_{OH} (V)	4.5	4.4987	-0.029
V_{OL} (V)	0	0	0

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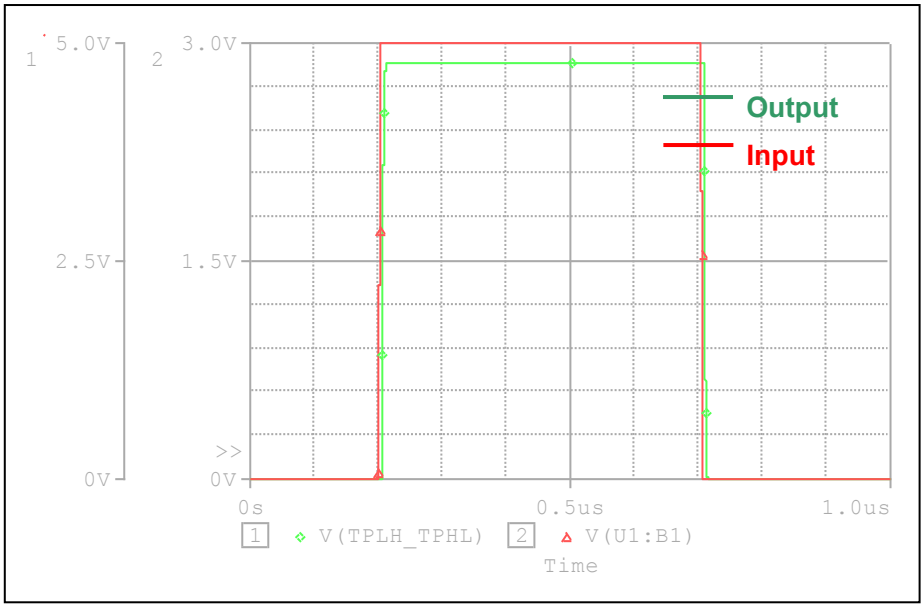
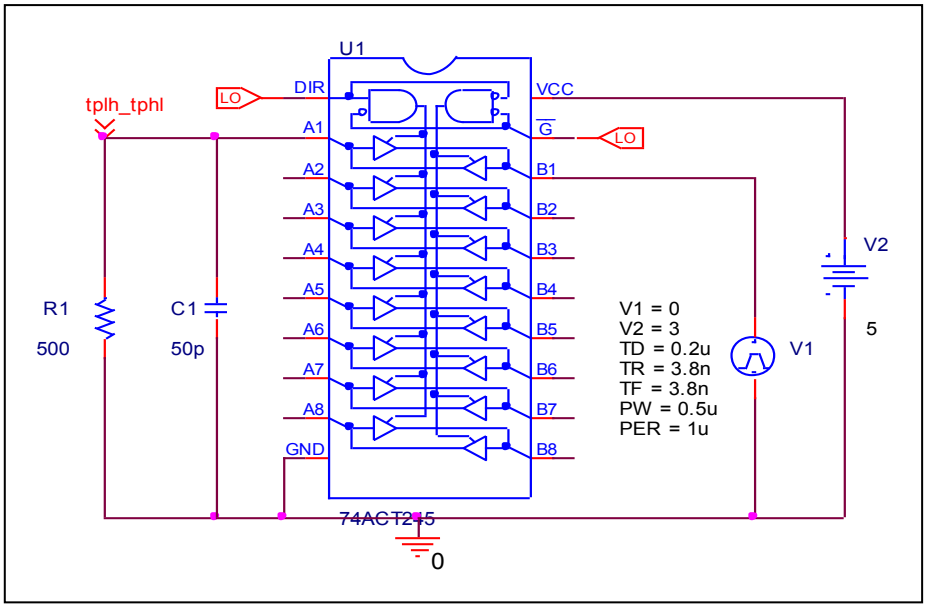
Propagation Delay Time

Circuit simulation result



Evaluation circuit



Comparison table C_L = 50 pF, R_L = 500 Ω

$t_r = t_f$ =3 ns	Measurement	Simulation	%Error
t_{PLH} (ns)	5	5.0128	0.256
t_{PHL} (ns)	5	5.014	0.280

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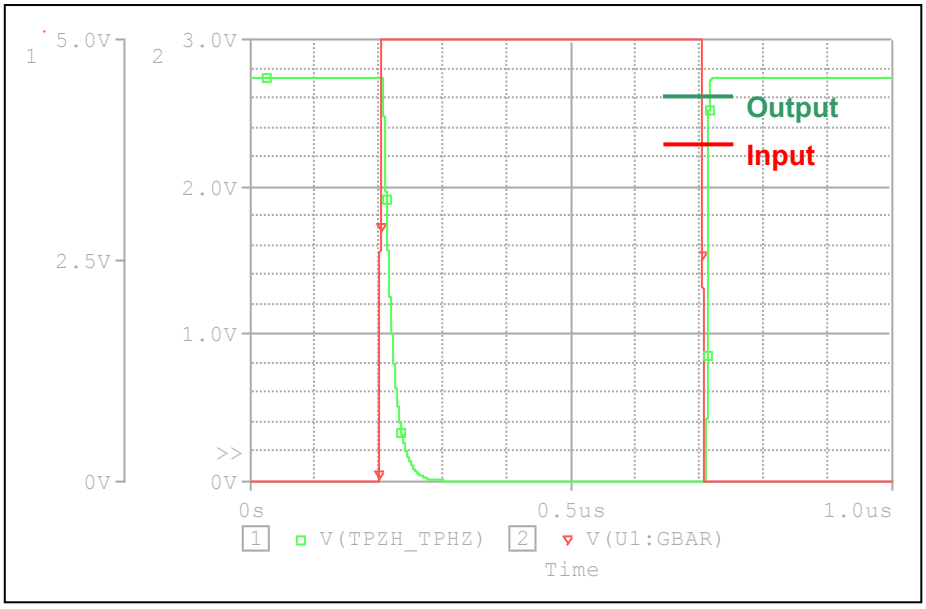
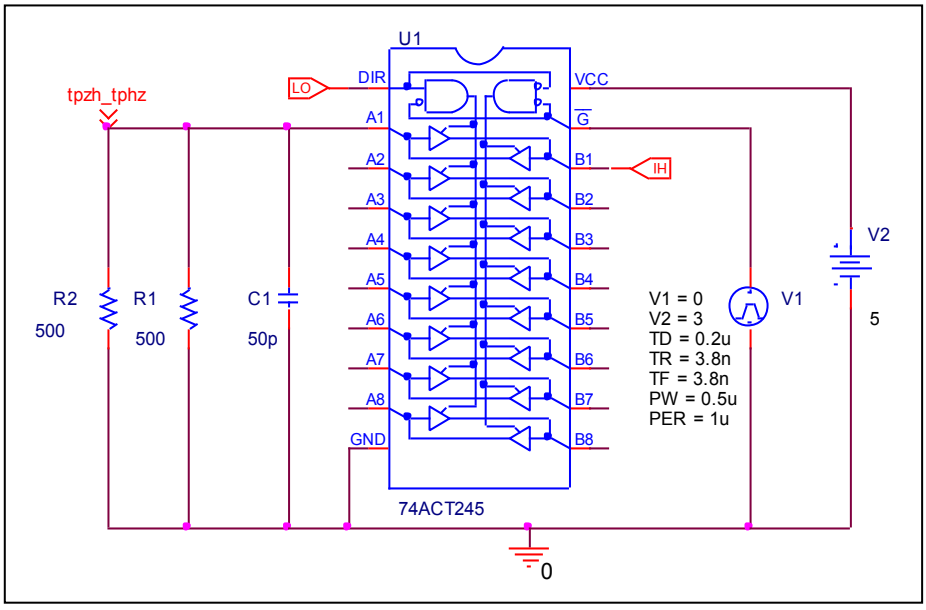
Output enable time, high impedance (off) to high output (t_{PZH})
Output disable time, high to high impedance (off) output (t_{PHZ})

Circuit simulation result



Evaluation circuit



Comparison table C_L = 50 pF, R_L = 500 Ω

$t_r = t_f$ =3 ns	Measurement	Simulation	%Error
t_{PZH} (ns)	7.3	7.3756	1.036
t_{PHZ} (ns)	6.3	6.3548	0.870

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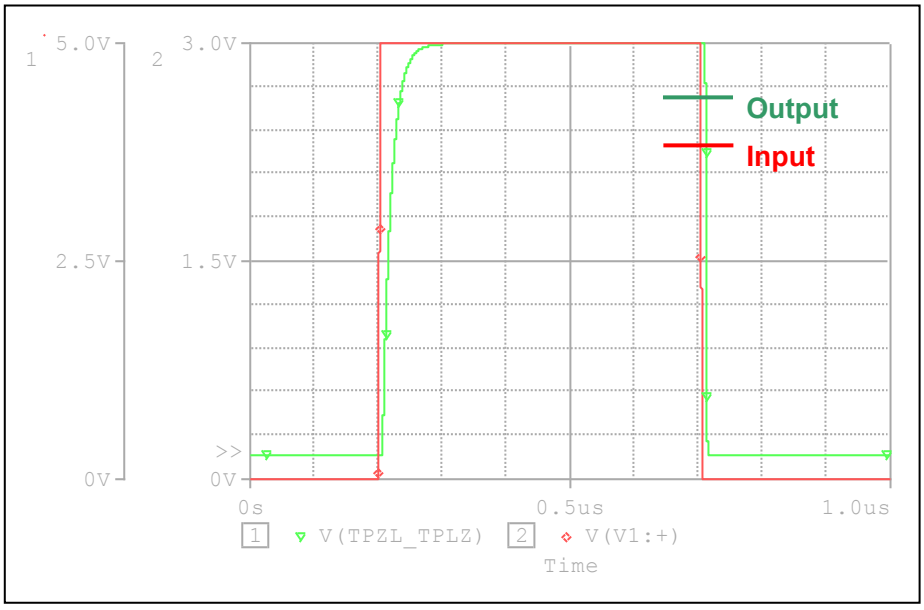
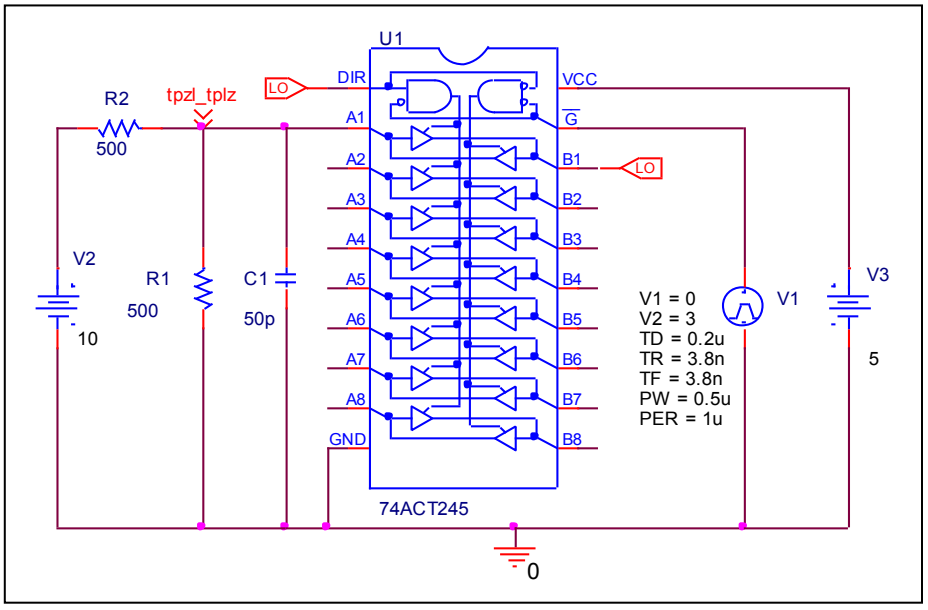
Output enable time, high impedance (off) to low output (t_{PZL})
Output disable time, low to high impedance (off) output (t_{PLZ})

Circuit simulation result



Evaluation circuit



Comparison table C_L = 50 pF, R_L = 500 Ω

$t_r = t_f$ =3 ns	Measurement	Simulation	%Error
t_{PZL} (ns)	7.3	7.3644	0.882
t_{PLZ} (ns)	6.3	6.3547	0.868

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