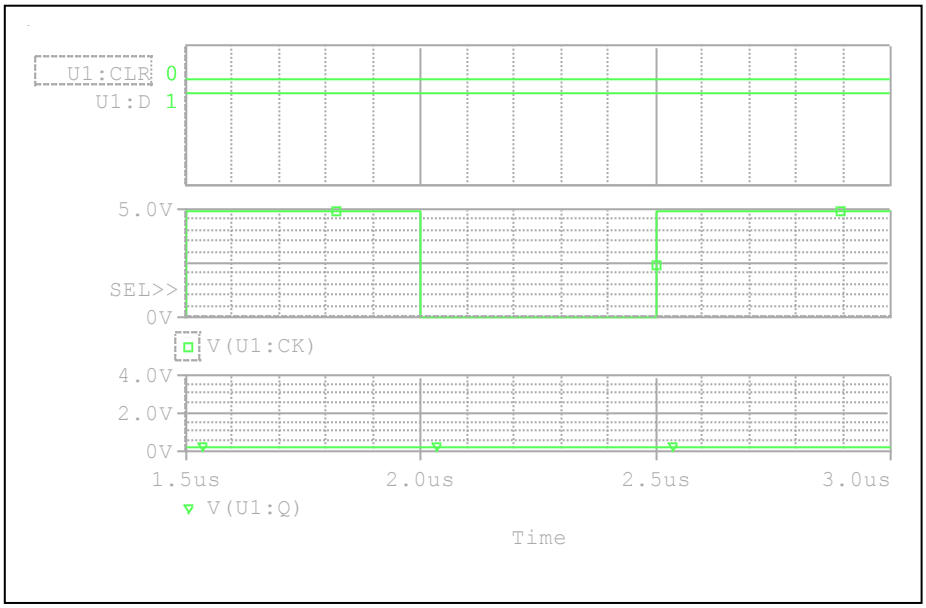
Device Modeling Report

COMPONENTS : CMOS DIGITAL INTEGRATED CIRCUIT
PART NUMBER : TC7PA175FU
MANUFACTURER : TOSHIBA

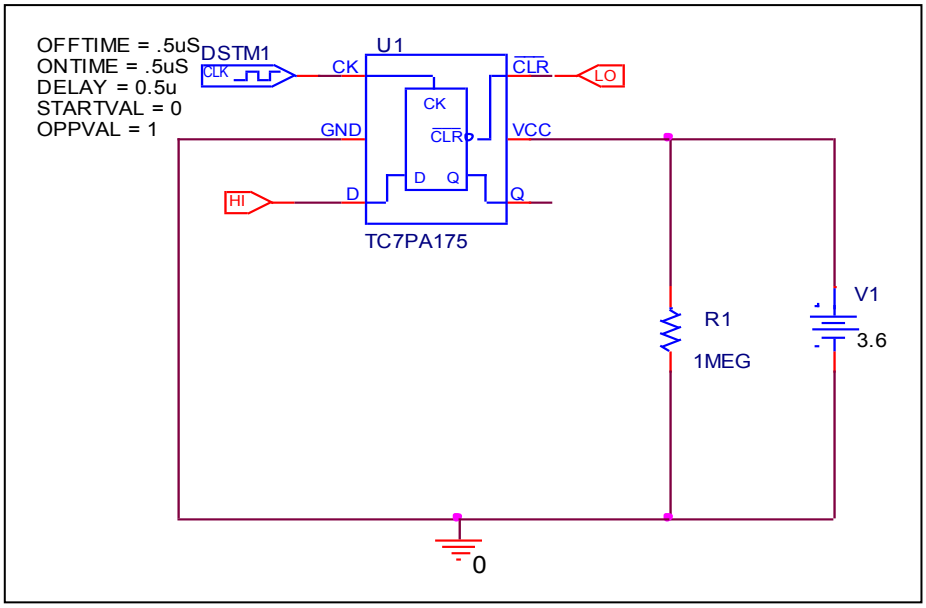
Bee Technologies Inc.

Truth Table

Circuit simulation result



Evaluation circuit

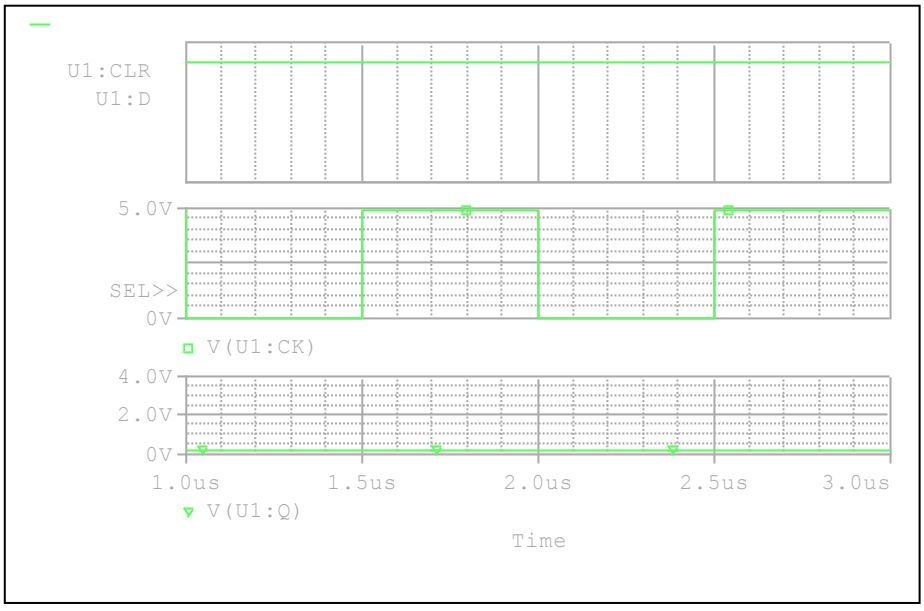


Comparison table

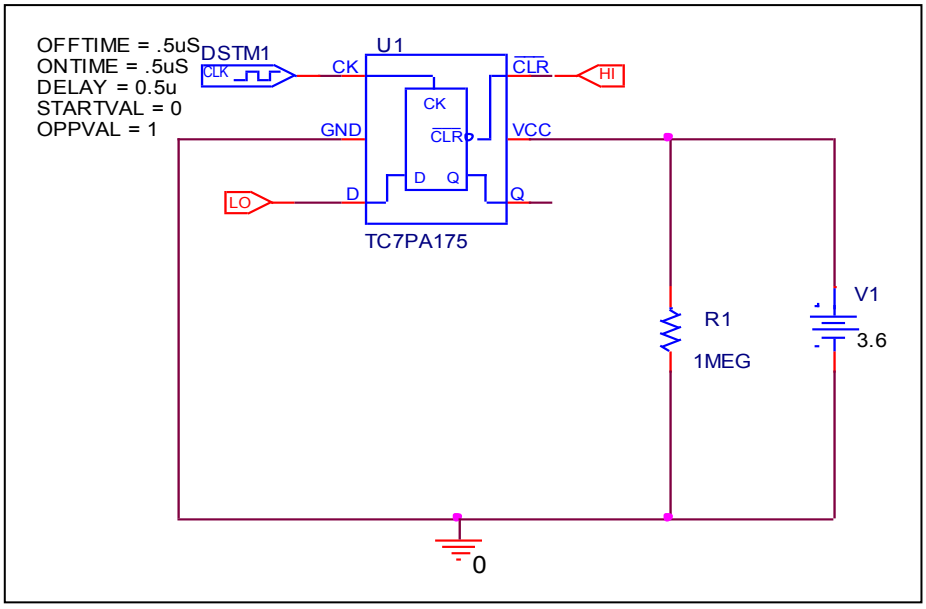
Input			OUTPUT Q		%Error
$\overline{CLR}$	D	CK	Measurement	Simulation	
L	X	X	L	L	0

Truth Table

Circuit simulation result



Evaluation circuit

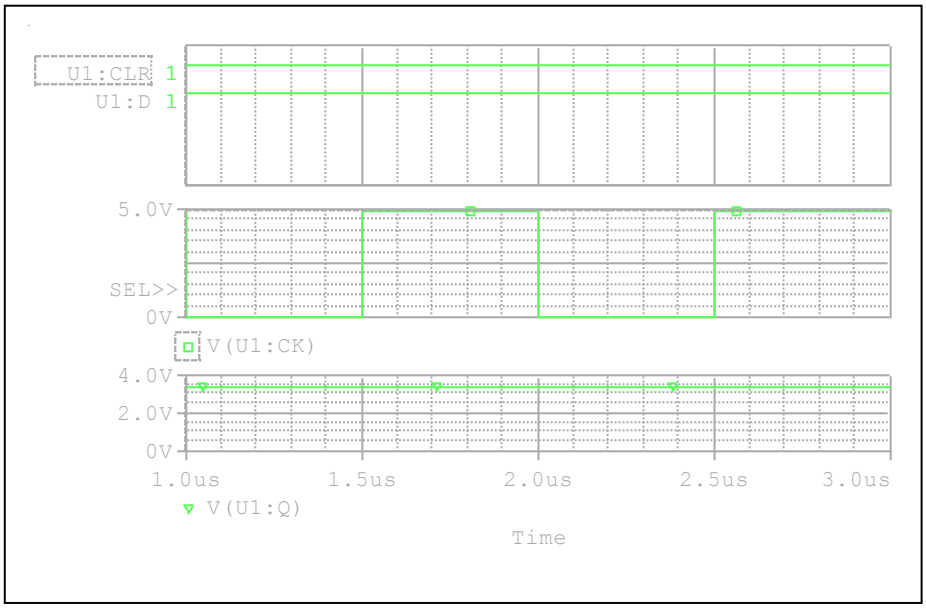


Comparison table

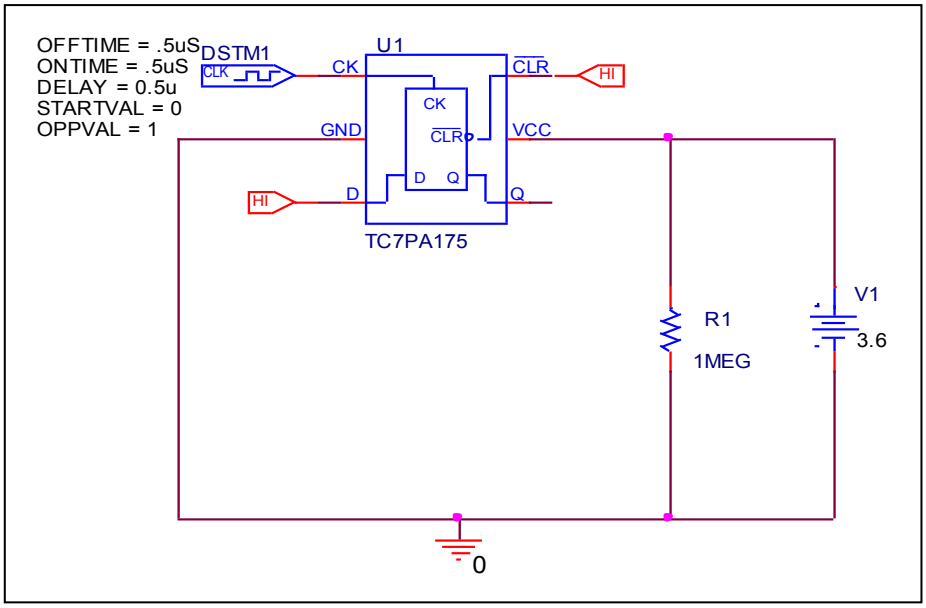
Input			OUTPUT Q		%Error
$\overline{CLR}$	D	CK	Measurement	Simulation	
H	L	↑	L	L	0

Truth Table

Circuit simulation result



Evaluation circuit

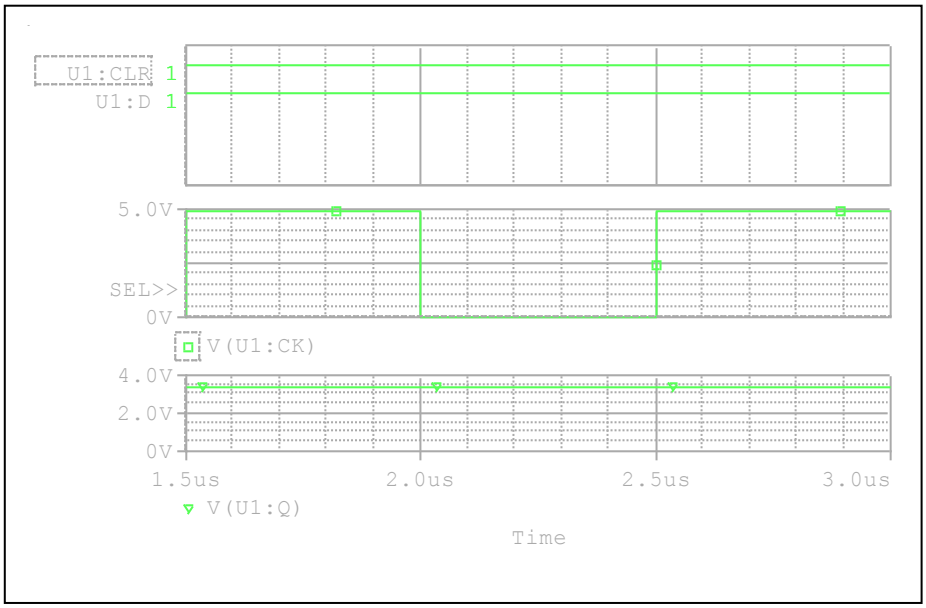


Comparison table

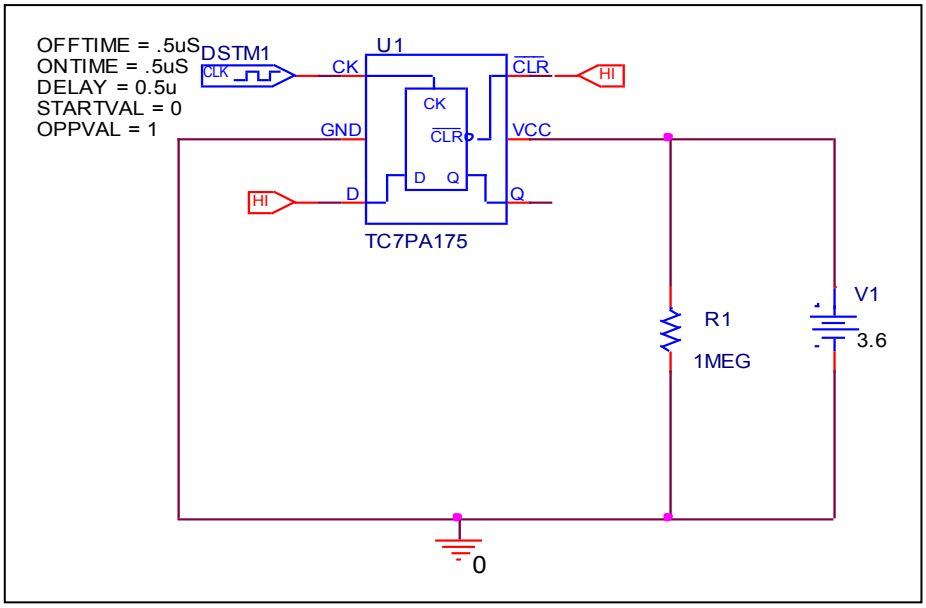
Input			OUTPUT Q		%Error
$\overline{CLR}$	D	CK	Measurement	Simulation	
H	H	↑	H	H	0

Truth Table

Circuit simulation result



Evaluation circuit

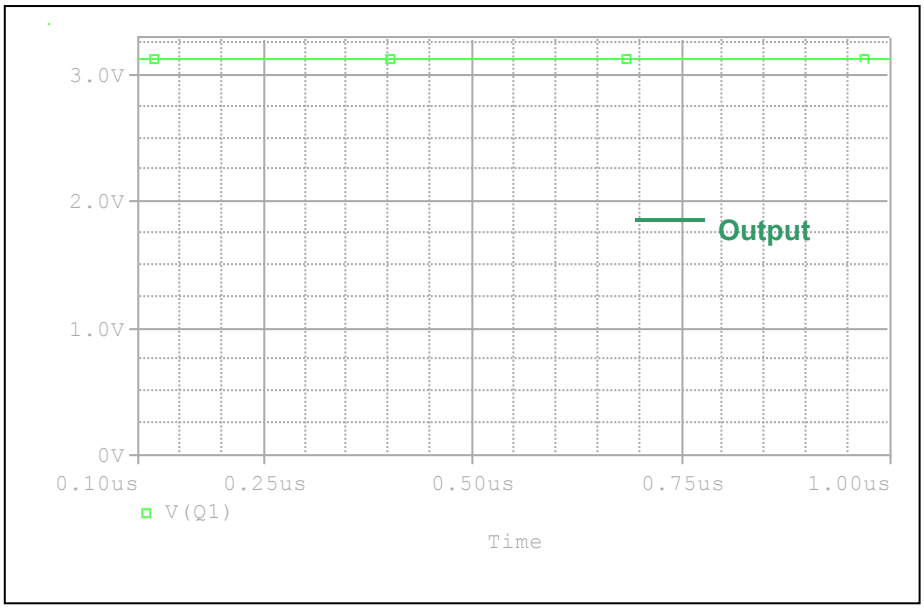


Comparison table

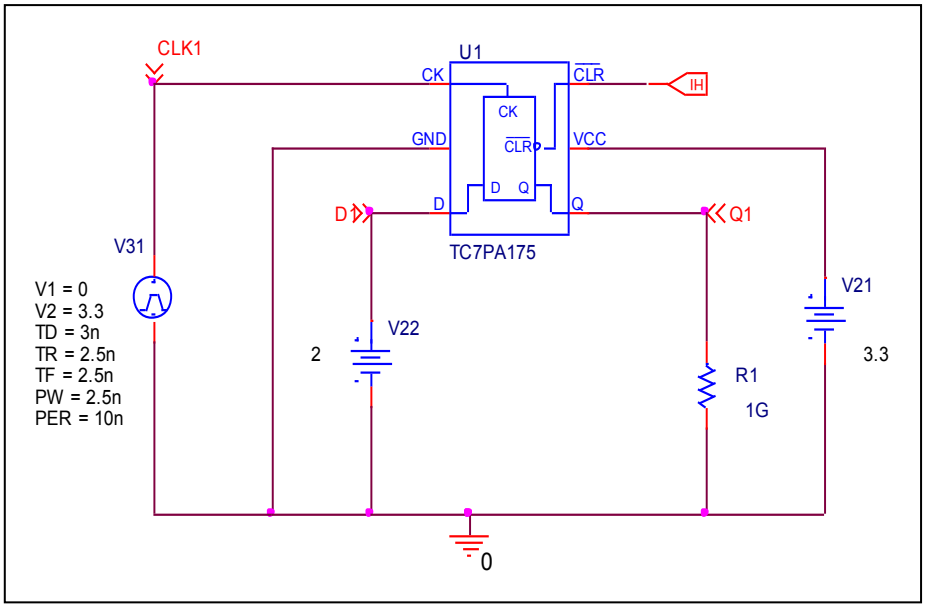
Input			OUTPUT Q		%Error
$\overline{CLR}$	D	CK	Measurement	Simulation	
H	X	↓	Qn	Qn	0

High Level Input Voltage (2.7 V < V_{CC} ≤ 3.6 V)

Circuit simulation result



Evaluation circuit

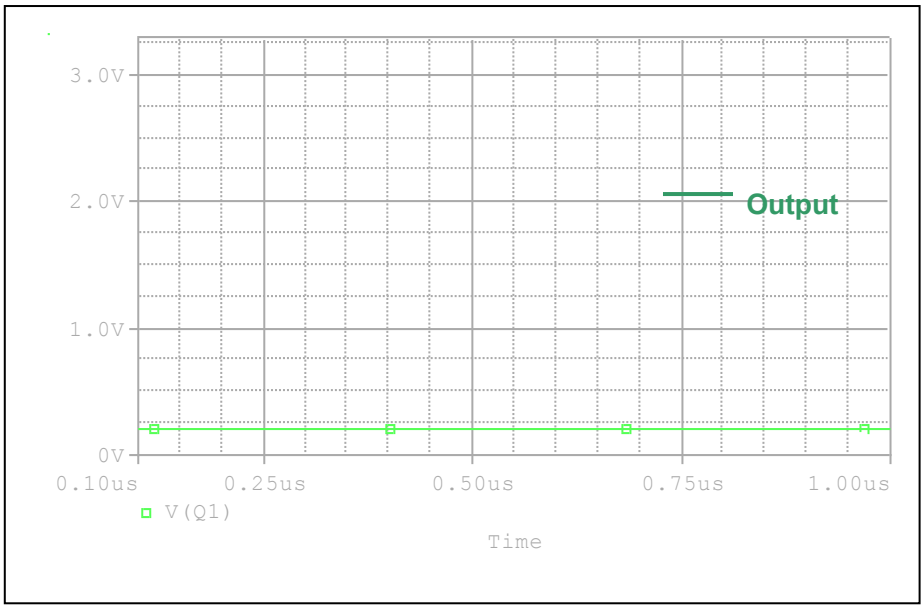


Comparison table

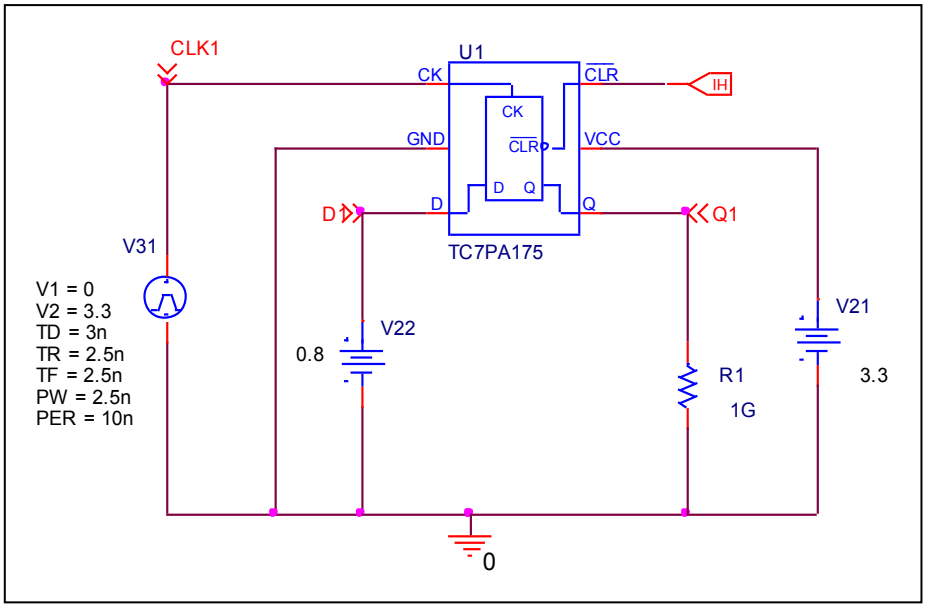
V_{CC} = 3.3 V	Measurement	Simulation	%Error
V_{IH} (V)	2	2	0

Low Level Input Voltage (2.7 V < V_{CC} ≤ 3.6 V)

Circuit simulation result



Evaluation circuit

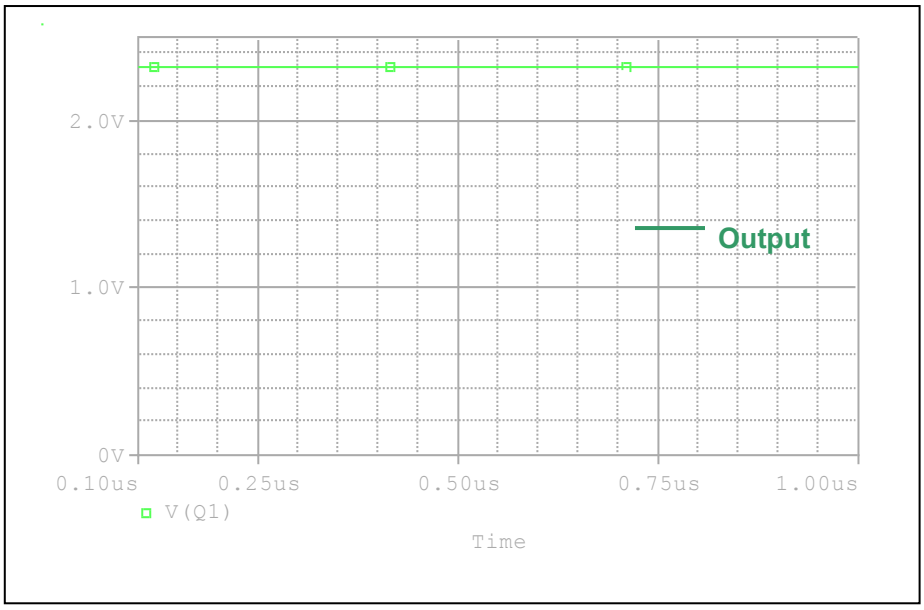


Comparison table

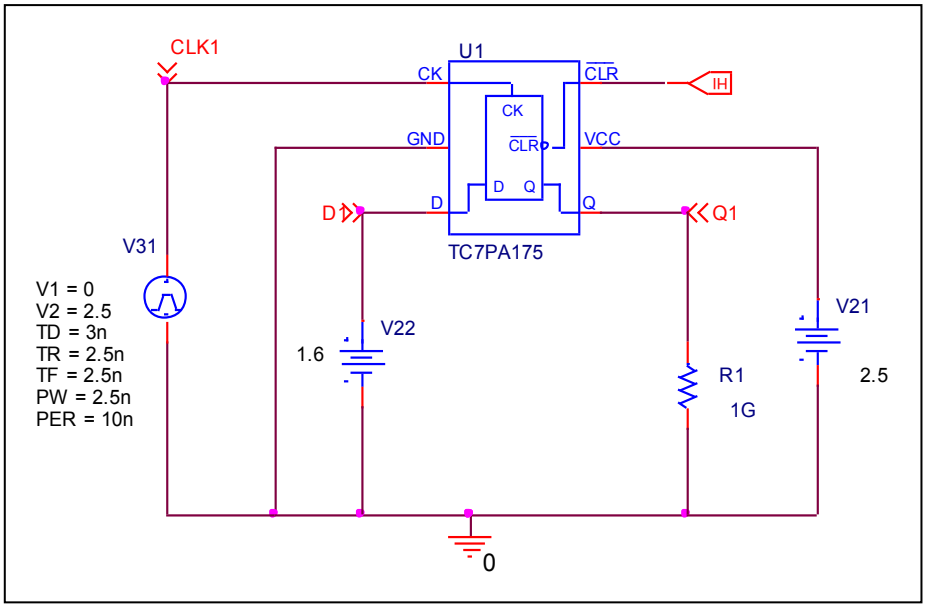
V_{CC} = 3.3 V	Measurement	Simulation	%Error
V_{IL} (V)	0.8	0.8	0

High Level Input Voltage (2.3 V ≤ V_{CC} ≤ 2.7 V)

Circuit simulation result



Evaluation circuit

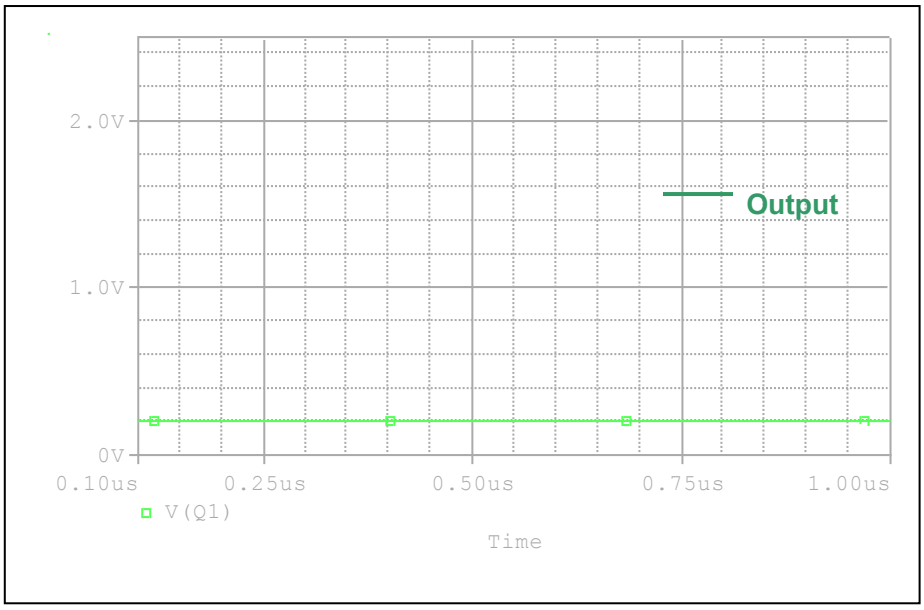


Comparison table

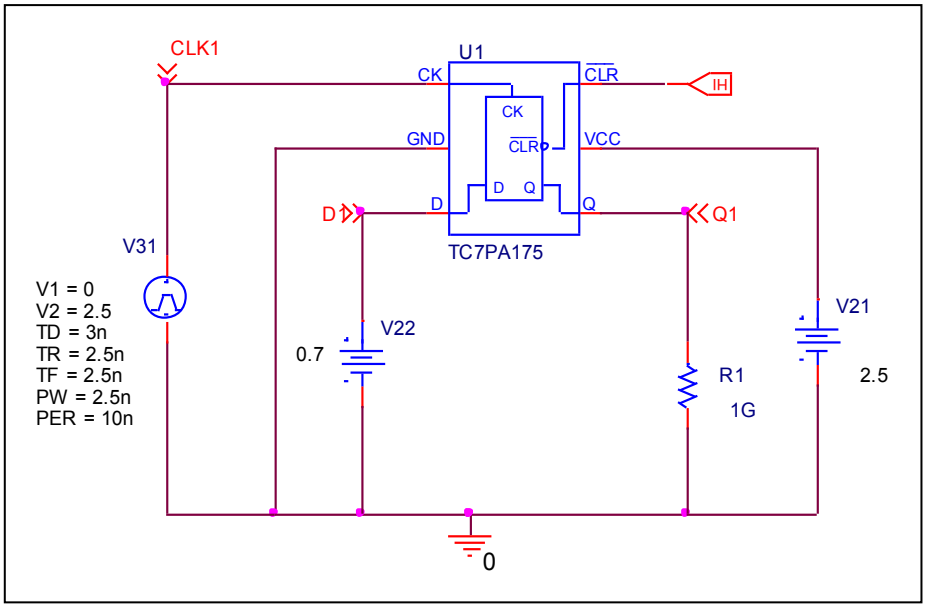
V_{CC} = 2.5 V	Measurement	Simulation	%Error
V_{IH} (V)	1.6	1.6	0

Low Level Input Voltage (2.3 V ≤ V_{CC} ≤ 2.7 V)

Circuit simulation result



Evaluation circuit

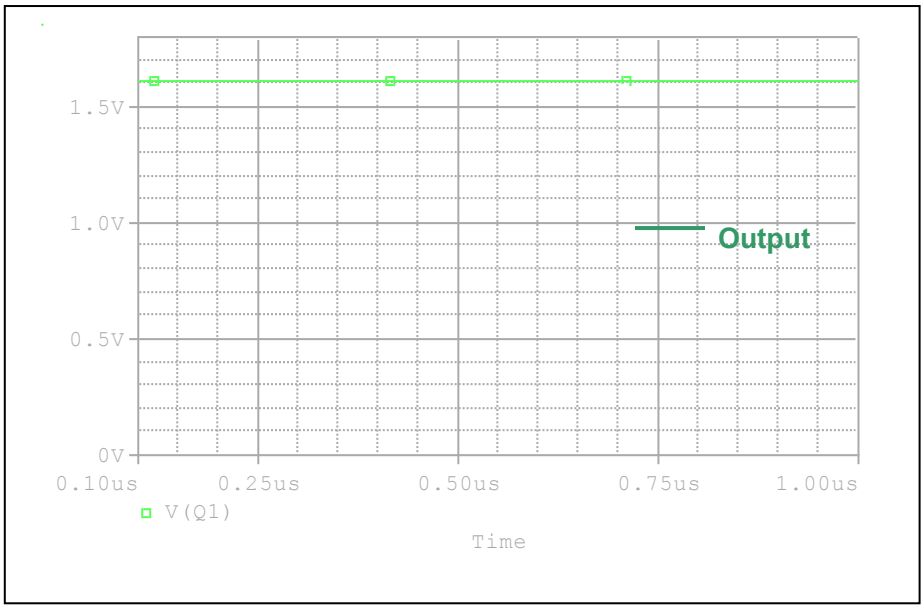


Comparison table

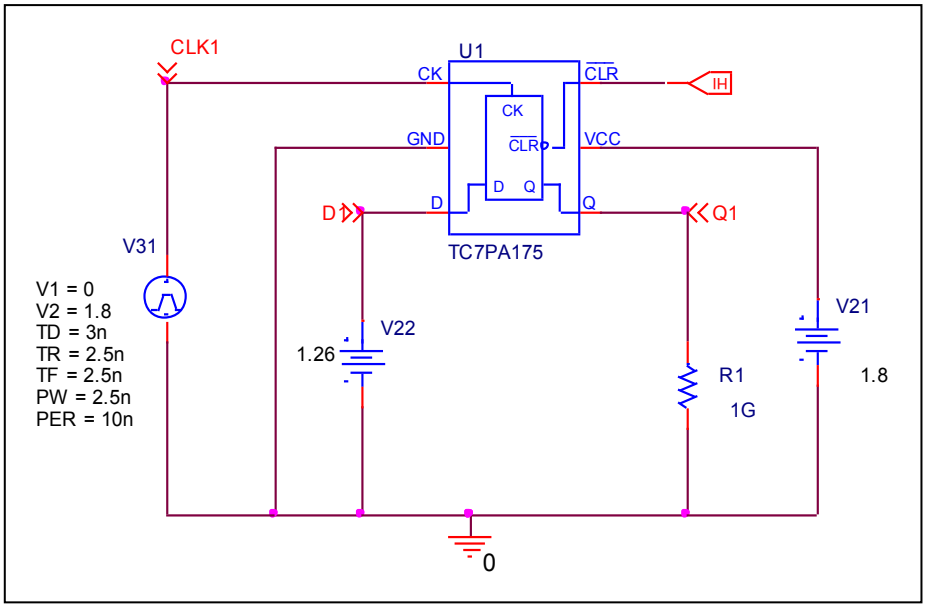
V_{CC} = 2.5 V	Measurement	Simulation	%Error
V_{IL} (V)	0.7	0.7	0

High Level Input Voltage (1.65 V ≤ V_{CC} < 2.3 V)

Circuit simulation result



Evaluation circuit

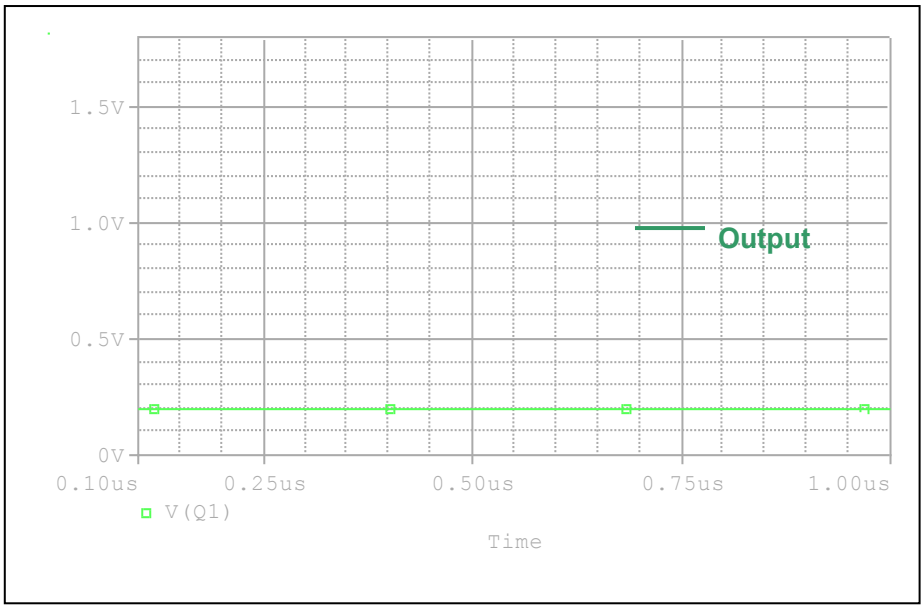


Comparison table

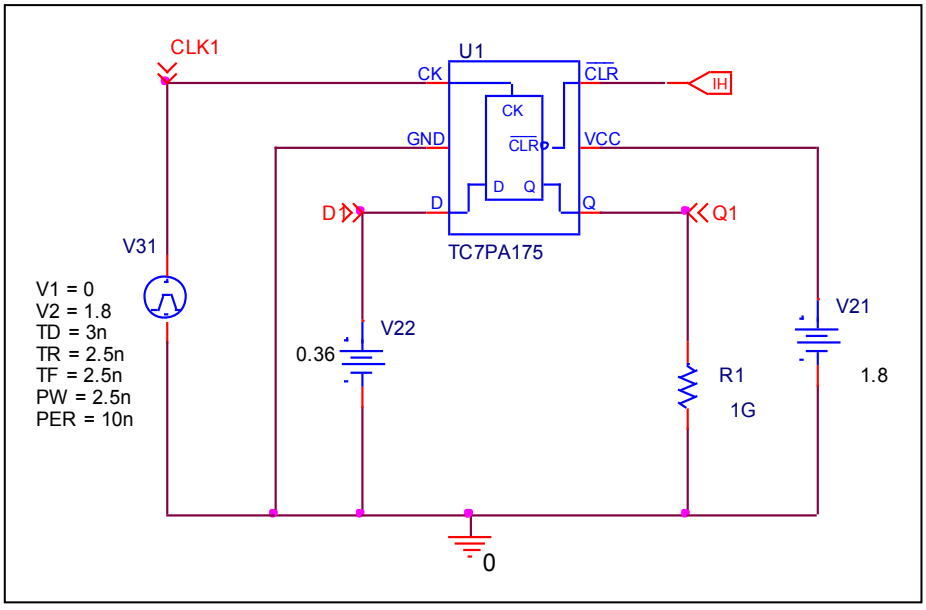
V_{CC} = 1.8 V	Measurement	Simulation	%Error
Min V_{IH} = (V_{CC}*0.7) (V)	1.26	1.26	0

Low Level Input Voltage (1.65 V ≤ V_{CC} < 2.3 V)

Circuit simulation result



Evaluation circuit

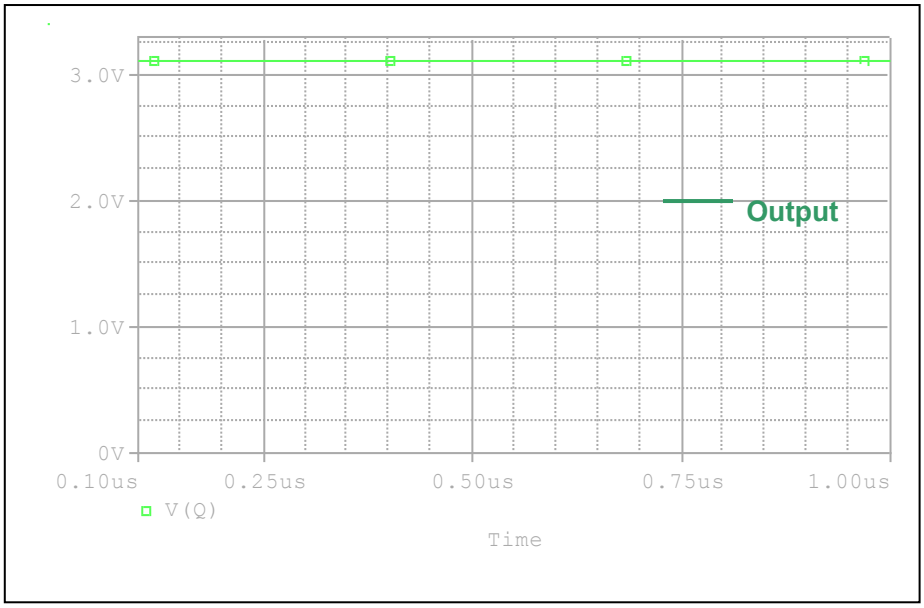


Comparison table

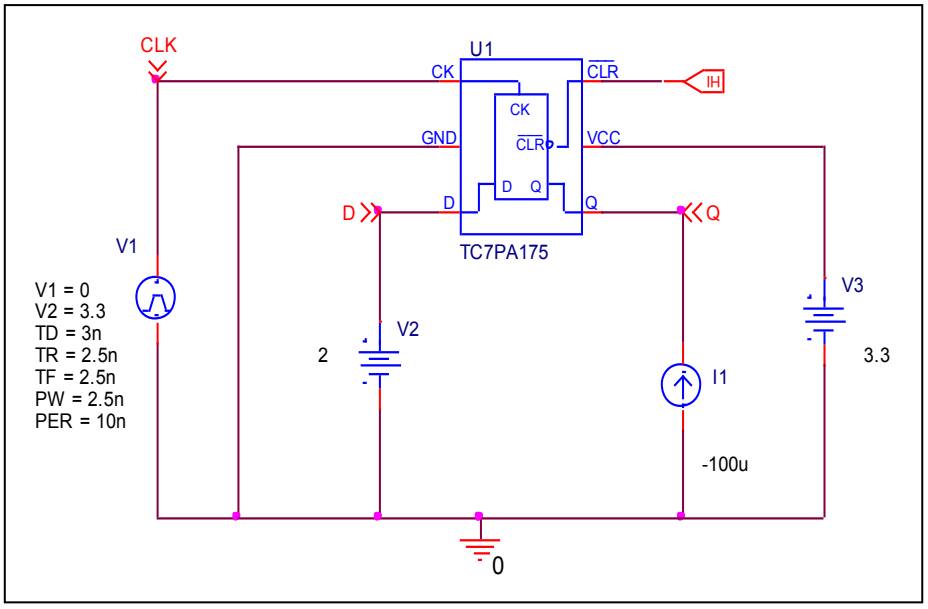
V_{CC} = 1.8 V	Measurement	Simulation	%Error
Max V_{IL} = (V_{CC}*0.2) (V)	0.36	0.36	0

High Level Output Voltage (2.7 V < V_{CC} ≤ 3.6 V)

Circuit simulation result



Evaluation circuit

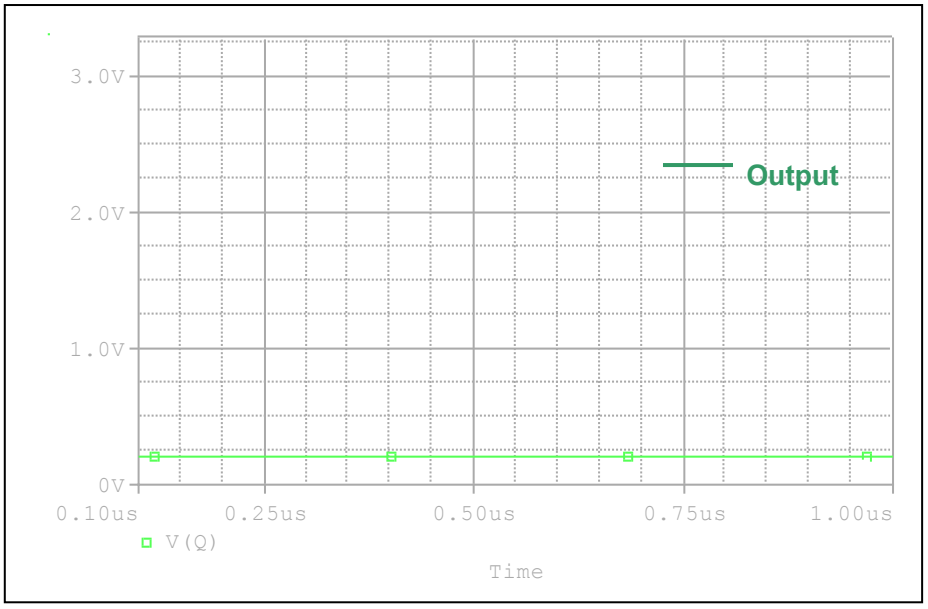


Comparison table

V_{CC} = 3.3 V	Measurement	Simulation	%Error
Min V_{OH} = (V_{CC} - 0.2) V	3.1	3.1162	0.523

Low Level Output Voltage (2.7 V < V_{CC} ≤ 3.6 V)

Circuit simulation result



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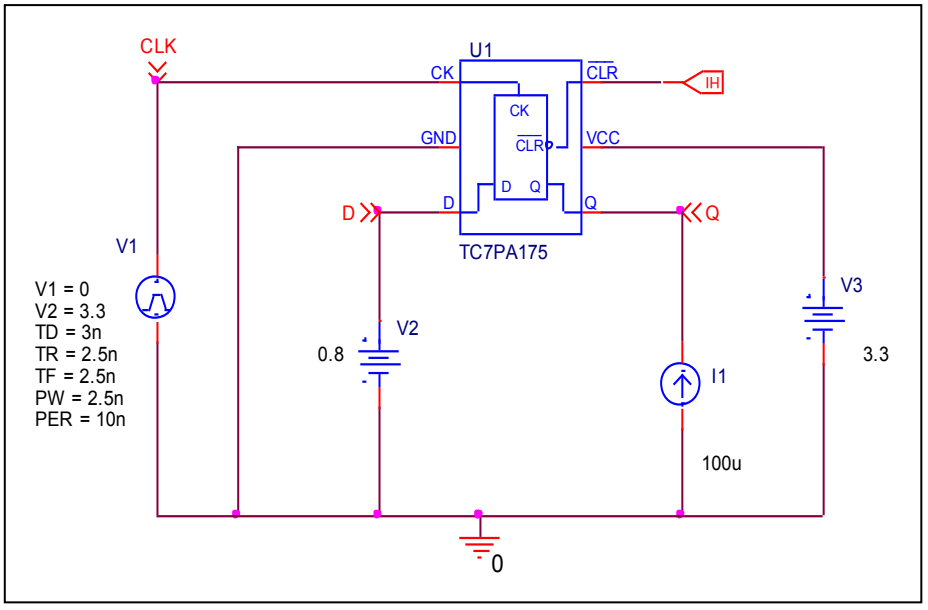
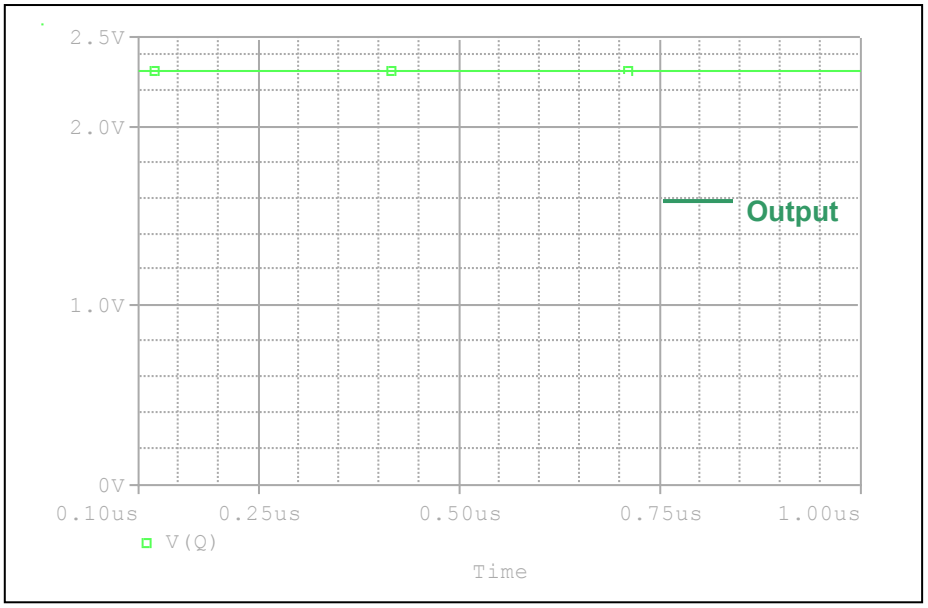


Comparison table

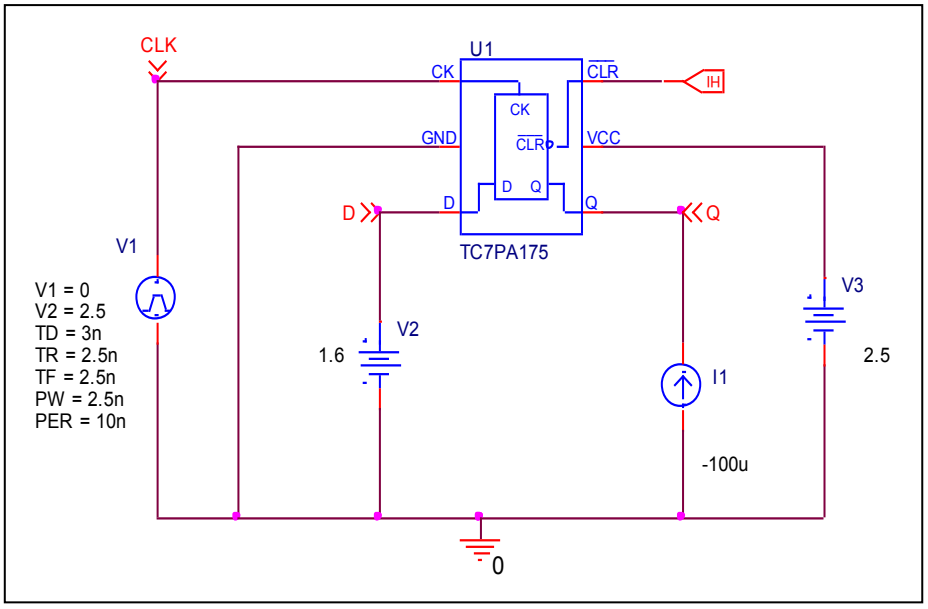
V_{CC} = 3.3 V	Measurement	Simulation	%Error
V_{OL} (V)	0.2	0.202436	1.218

High Level Output Voltage (2.3 V ≤ V_{CC} ≤ 2.7 V)

Circuit simulation result



Evaluation circuit

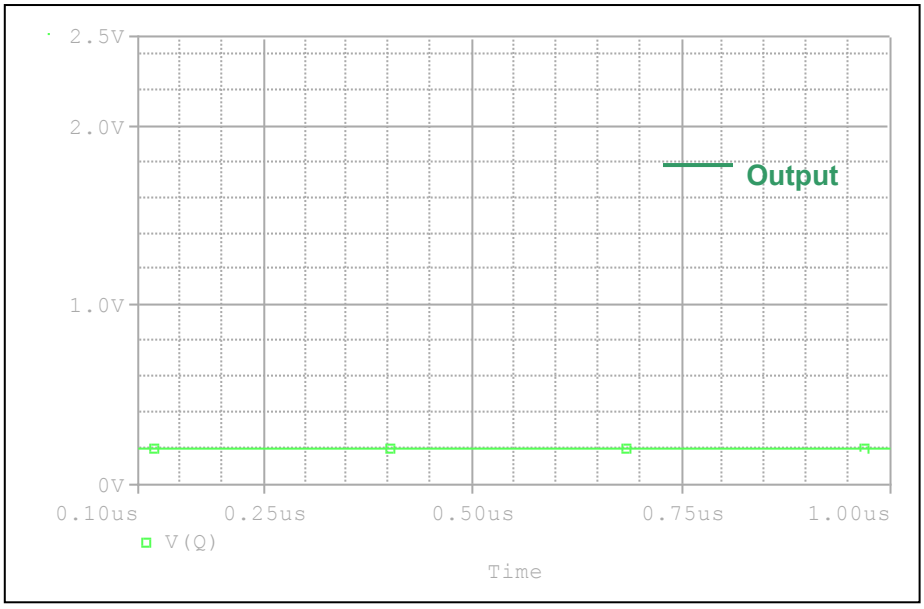


Comparison table

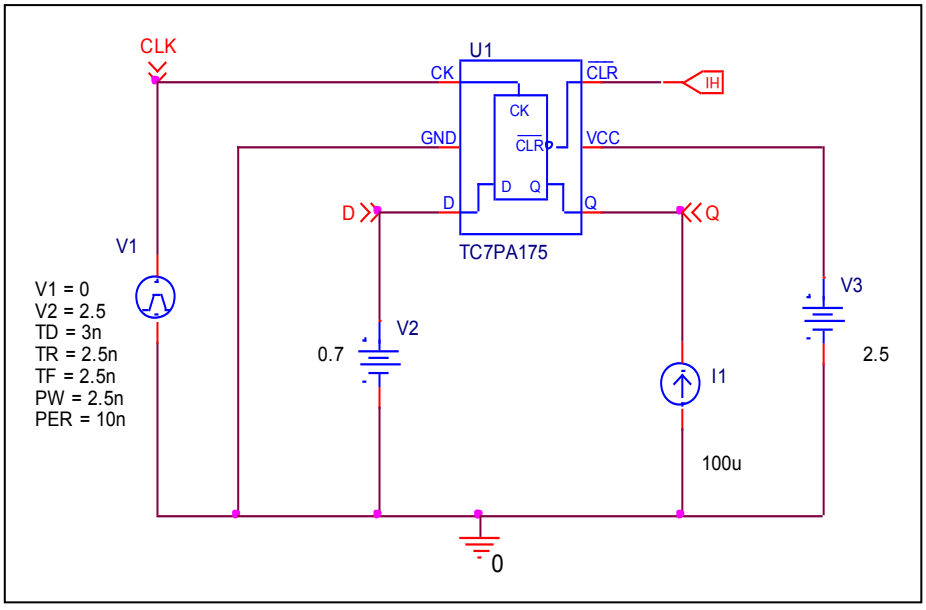
V_{CC} = 2.5 V	Measurement	Simulation	%Error
Min V_{OH} = (V_{CC} - 0.2) V	2.3	2.3156	0.678

Low Level Output Voltage (2.3 V ≤ V_{CC} ≤ 2.7 V)

Circuit simulation result



Evaluation circuit

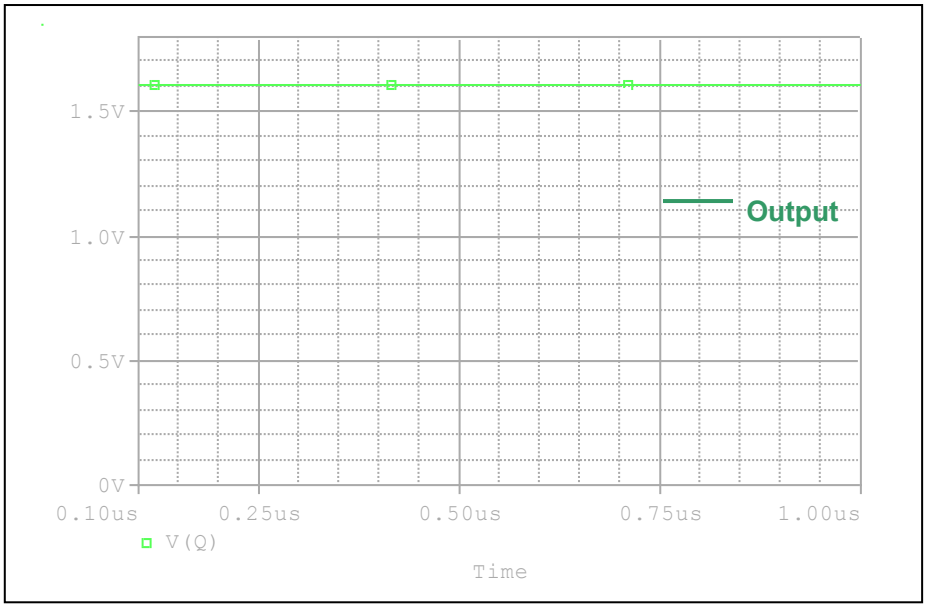


Comparison table

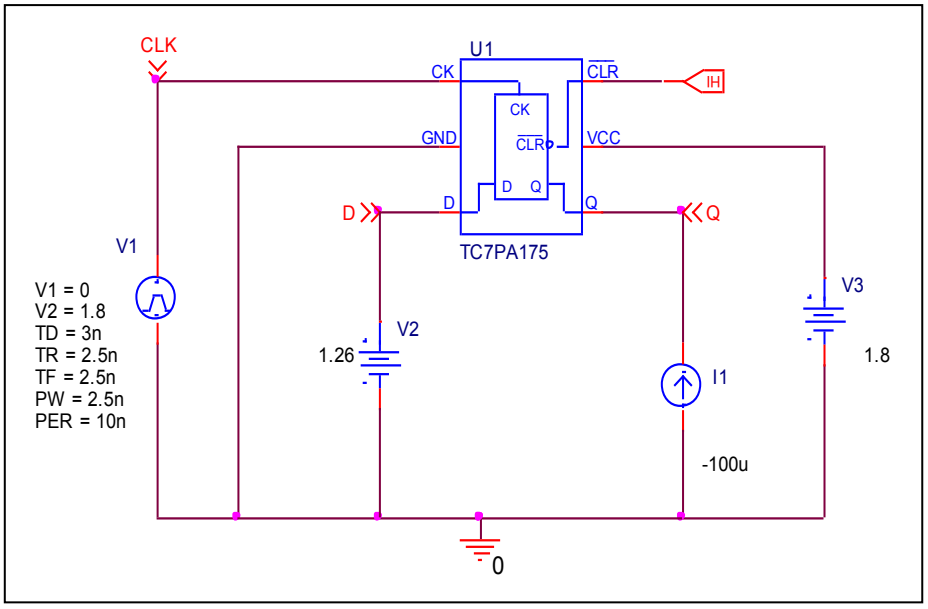
V_{CC} = 2.5 V	Measurement	Simulation	%Error
V_{OL} (V)	0.2	0.204523	2.262

High Level Output Voltage (1.8 V ≤ V_{CC} < 2.3 V)

Circuit simulation result



Evaluation circuit

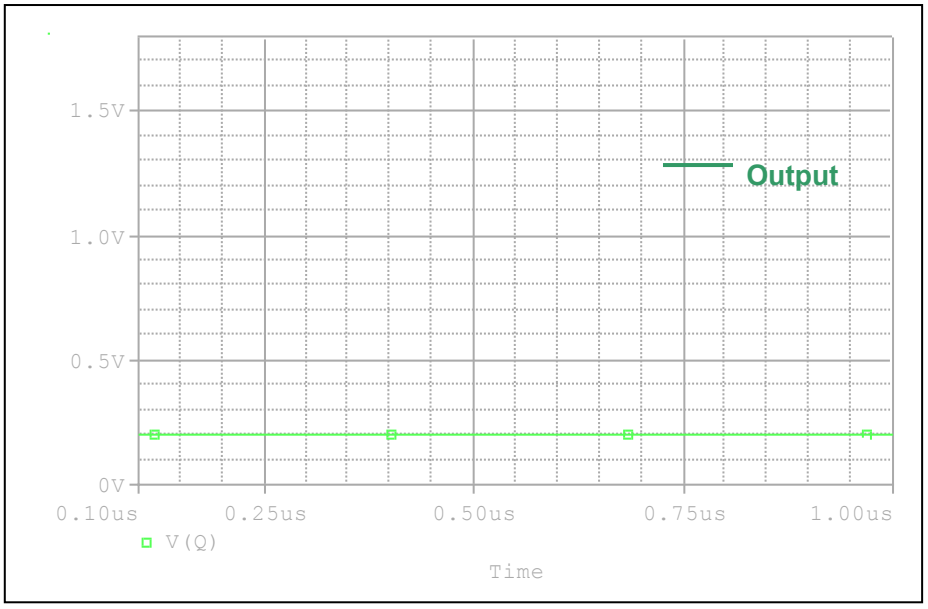


Comparison table

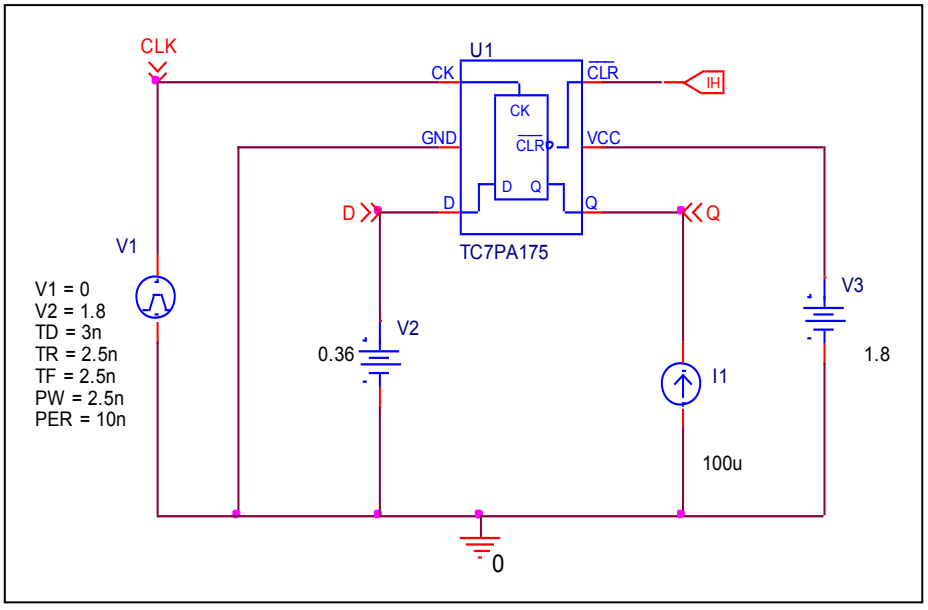
V_{CC} = 1.8 V	Measurement	Simulation	%Error
Min V_{OH} = (V_{CC} - 0.2) V	1.6	1.6062	0.387

Low Level Output Voltage (1.8 V ≤ V_{CC} < 2.3 V)

Circuit simulation result



Evaluation circuit

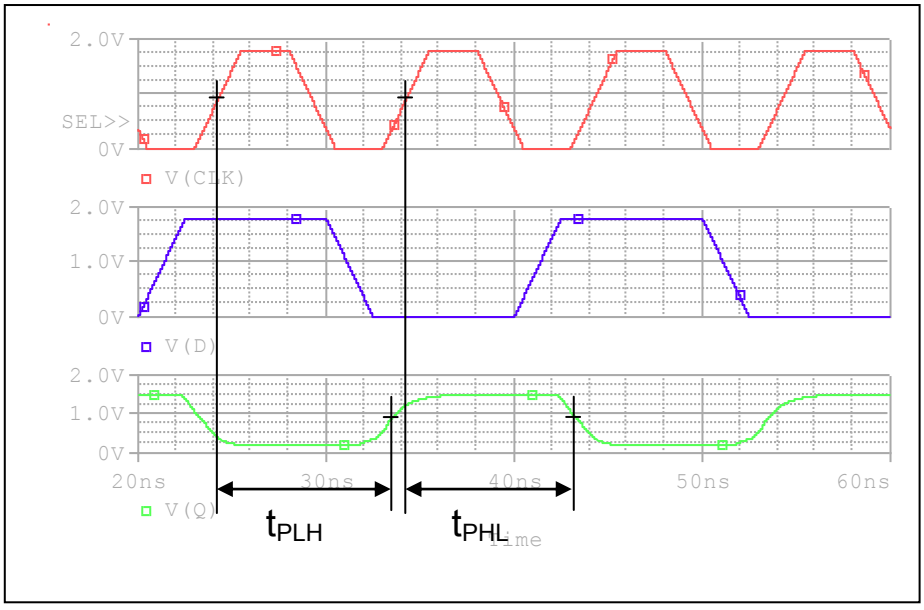


Comparison table

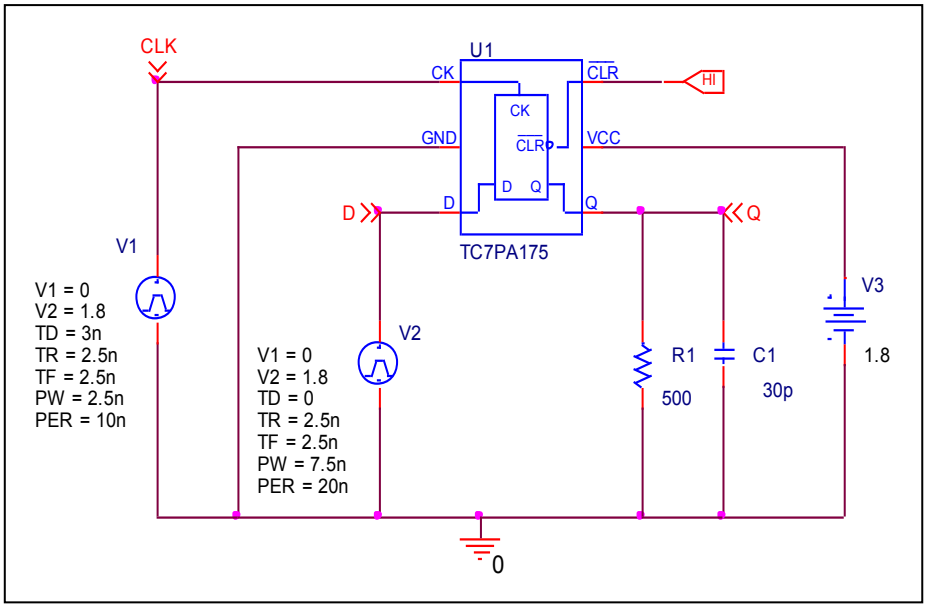
V_{CC} = 1.8 V	Measurement	Simulation	%Error
V_{OL} (V)	0.2	0.198028	-0.986

Propagation Delay Time (V_{CC} = 1.8 V, CK-Q)

Circuit simulation result



Evaluation circuit

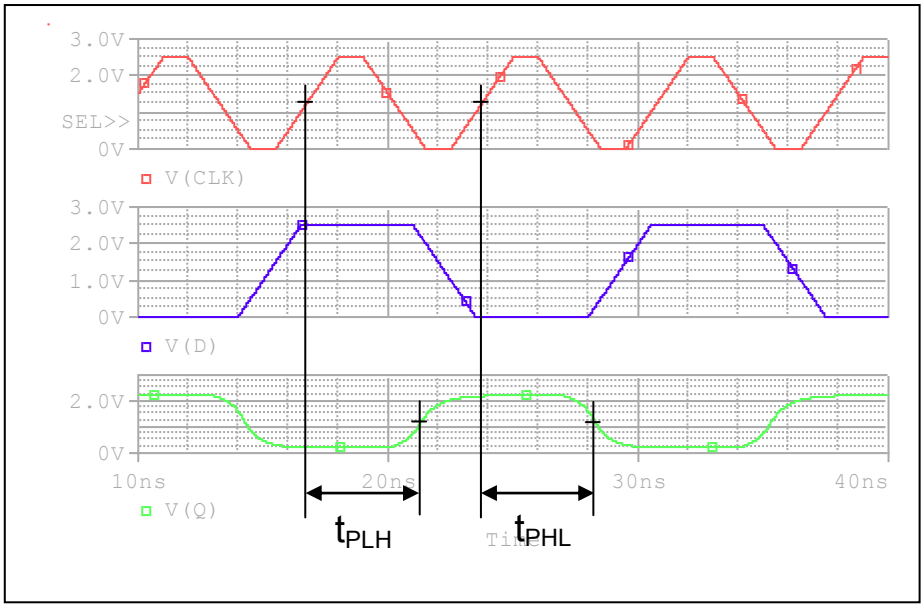


Comparison table C_L = 30 pF, R_L = 500 Ω

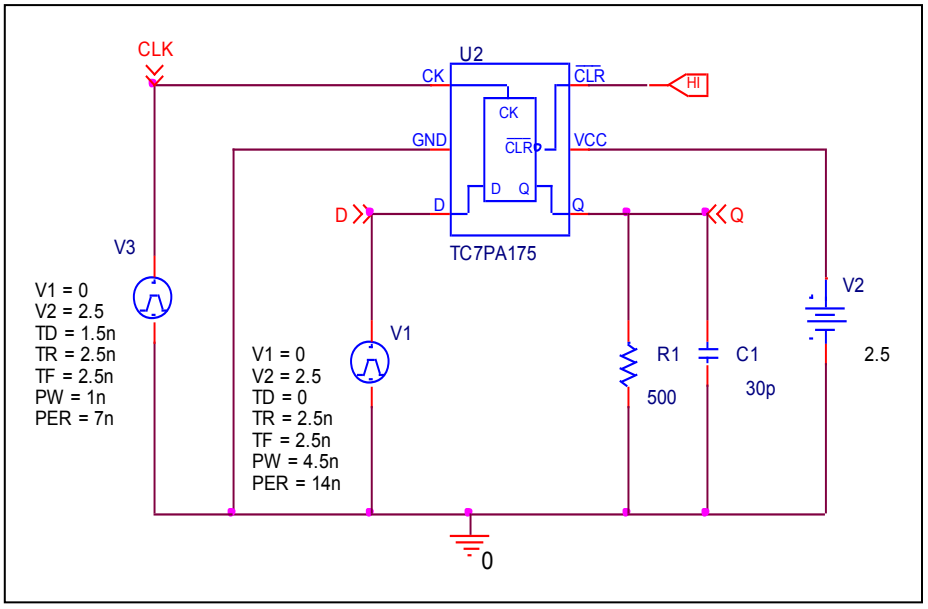
$t_r = t_f$ =2 ns	Measurement	Simulation	%Error
t_{PLH} (ns)	9.2	9.1611	-0.423
t_{PHL} (ns)	9.2	9.1576	-0.461

Propagation Delay Time (V_{CC} = 2.5 V, CK-Q)

Circuit simulation result



Evaluation circuit

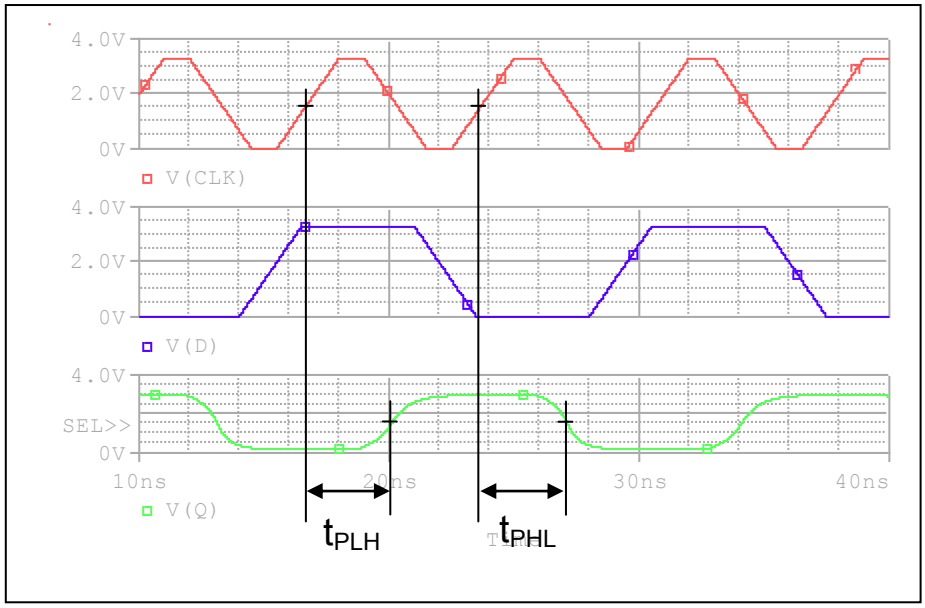


Comparison table C_L = 30 pF, R_L = 500 Ω

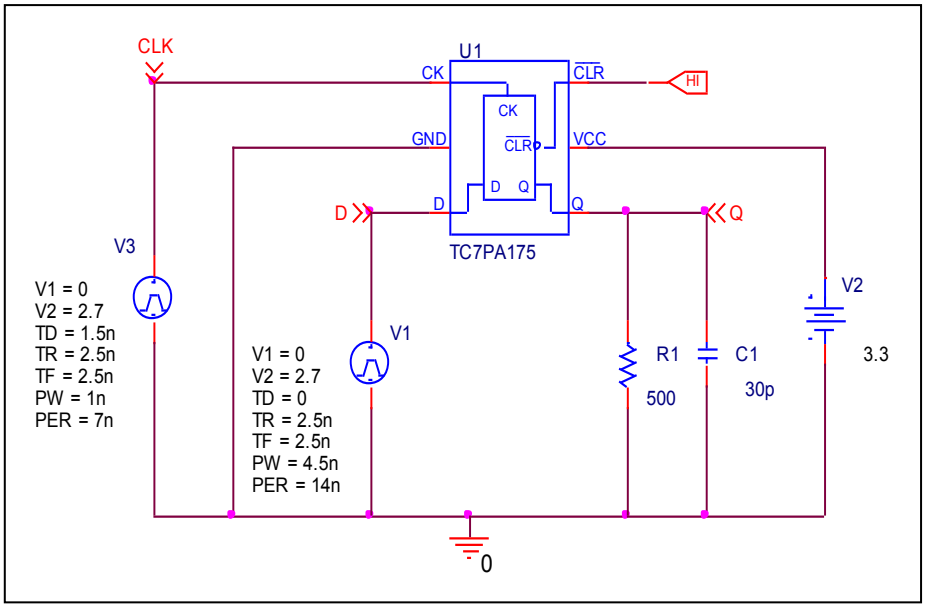
$t_r = t_f$ = 2 ns	Measurement	Simulation	%Error
t_{PLH} (ns)	4.6	4.5742	-0.561
t_{PHL} (ns)	4.6	4.5154	-1.839

Propagation Delay Time (V_{CC} = 3.3 V, CK-Q)

Circuit simulation result



Evaluation circuit

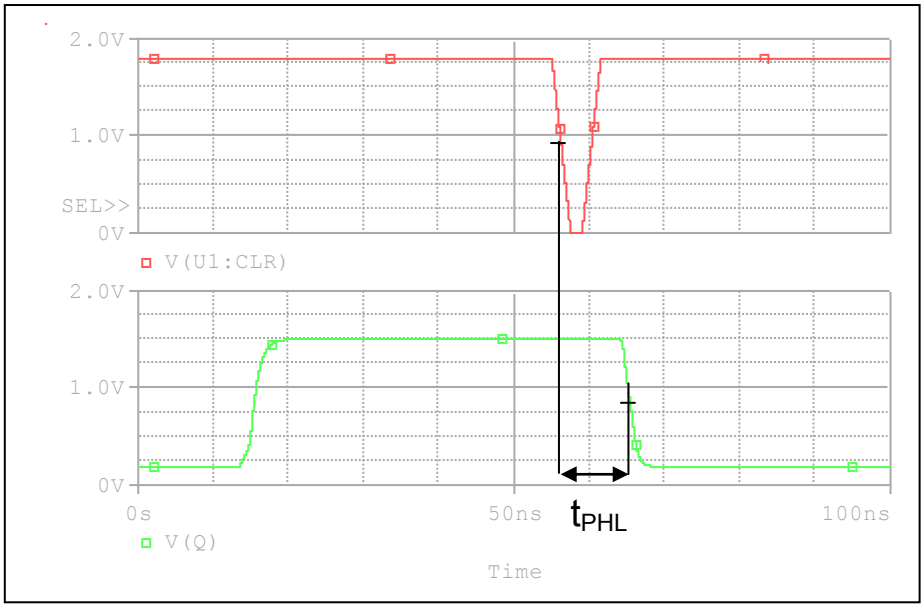


Comparison table C_L = 30 pF, R_L = 500 Ω

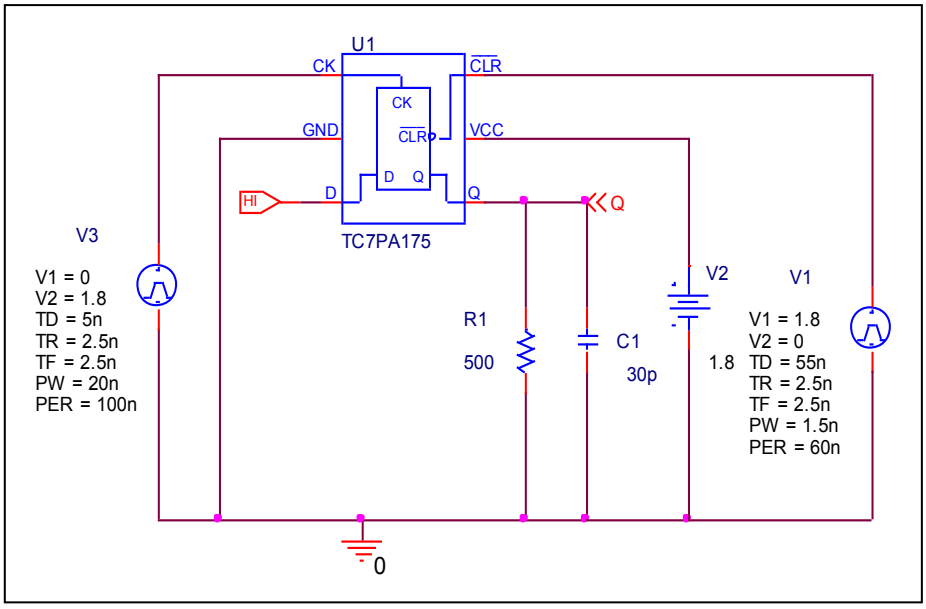
$t_r = t_f$ = 2 ns	Measurement	Simulation	%Error
t_{PLH} (ns)	3.5	3.4162	-2.394
t_{PHL} (ns)	3.5	3.4601	-1.140

Propagation Delay Time (V_{CC} = 1.8 V, $\overline{CLR}$ -Q)

Circuit simulation result



Evaluation circuit

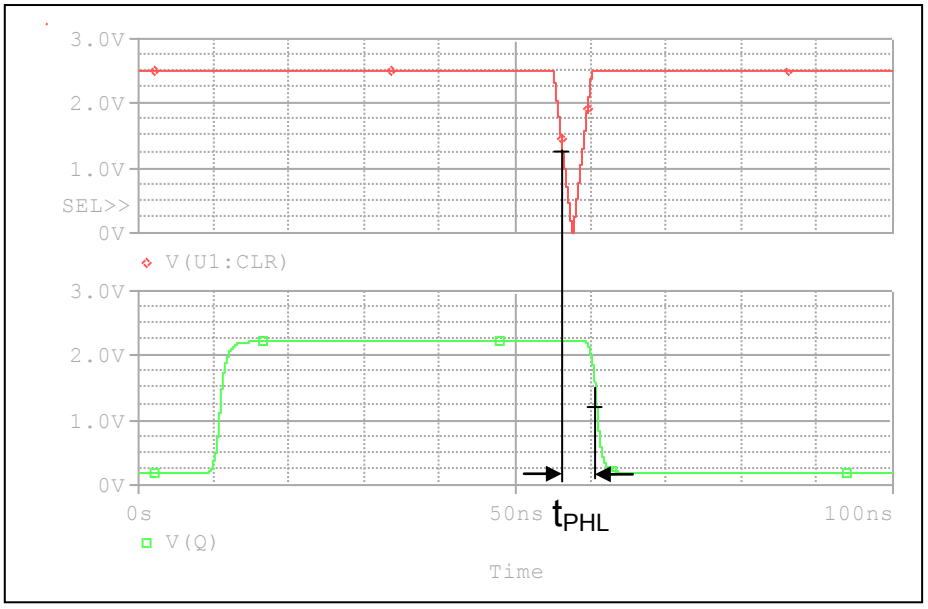


Comparison table C_L = 30 pF, R_L = 500 Ω

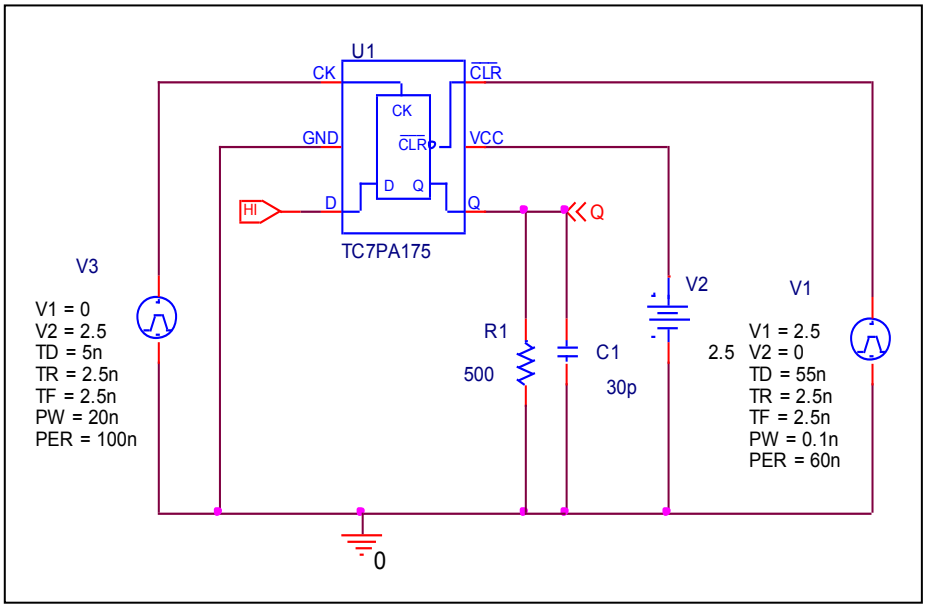
$t_r = t_f$ = 2 ns	Measurement	Simulation	%Error
t_{PHL} (ns)	9.2	9.1557	-0.482

Propagation Delay Time (V_{CC} = 2.5 V, $\overline{CLR}$ -Q)

Circuit simulation result



Evaluation circuit

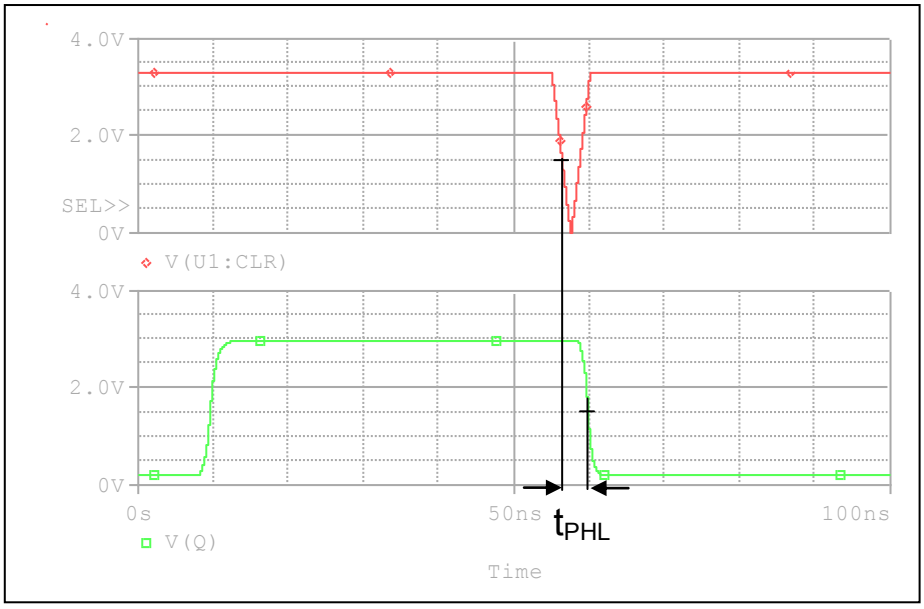


Comparison table C_L = 30 pF, R_L = 500 Ω

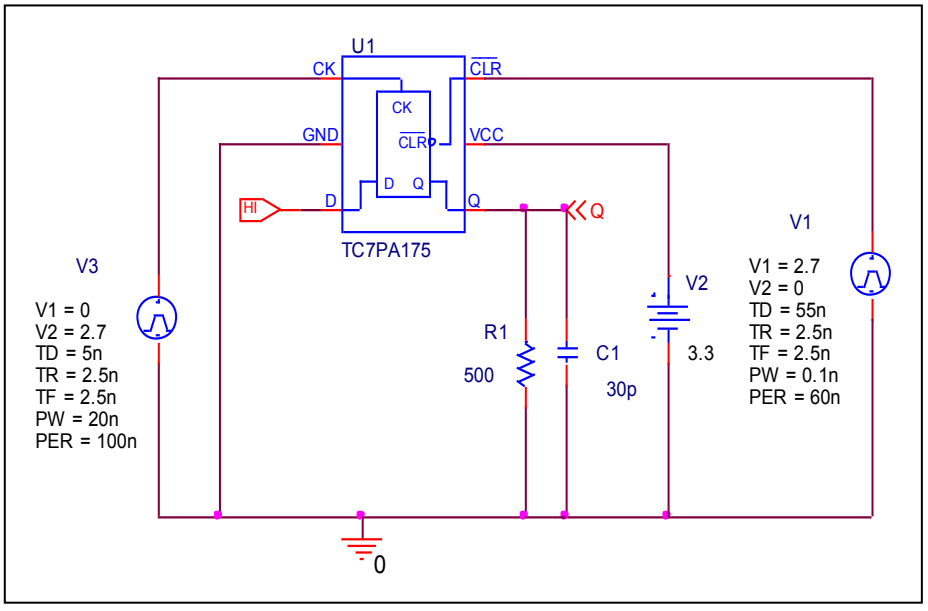
$t_r = t_f$ = 2 ns	Measurement	Simulation	%Error
t_{PHL} (ns)	4.6	4.5149	-1.850

Propagation Delay Time (V_{CC} = 3.3 V, $\overline{CLR}$ -Q)

Circuit simulation result



Evaluation circuit

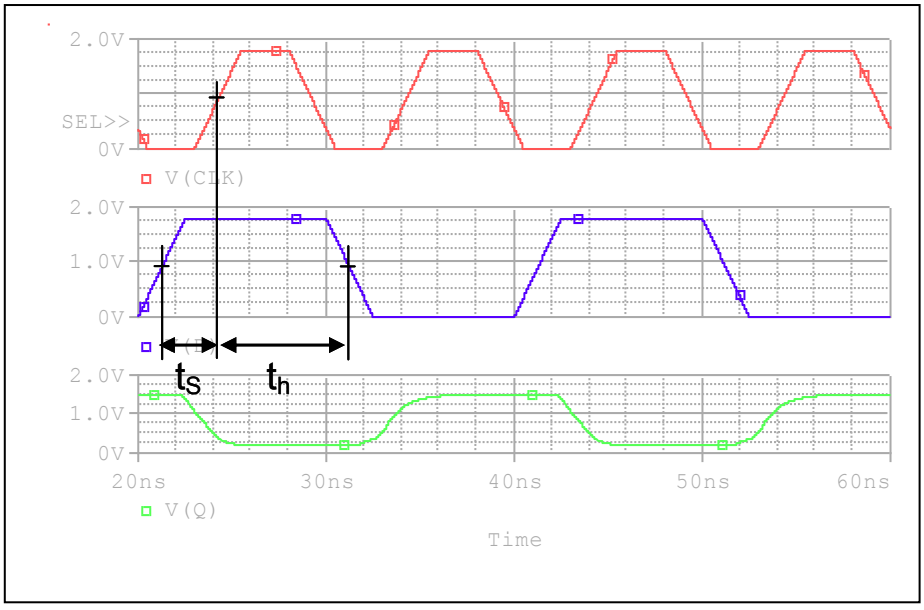


Comparison table C_L = 30 pF, R_L = 500 Ω

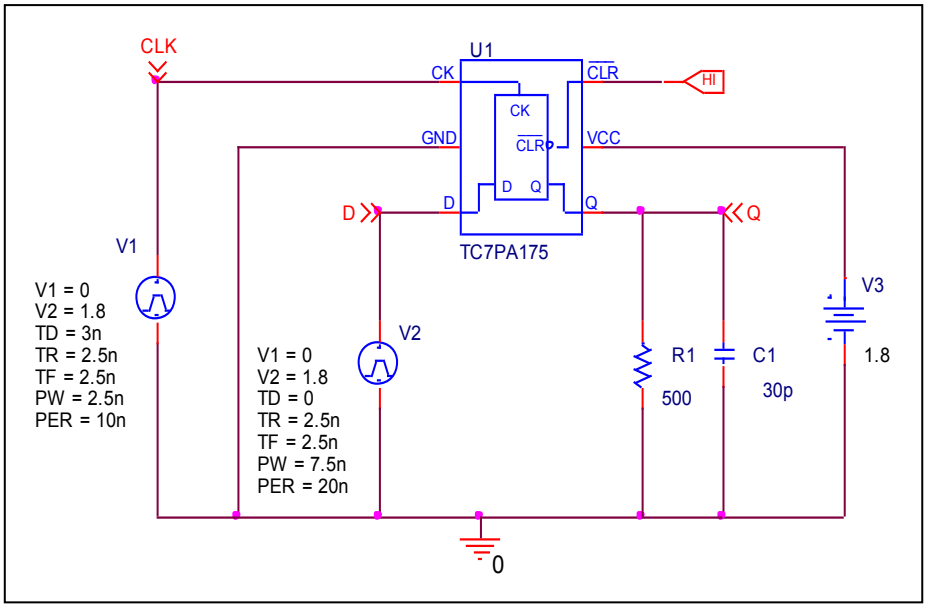
$t_r = t_f$ = 2 ns	Measurement	Simulation	%Error
t_{PHL} (ns)	3.5	3.494	-0.171

Minimum Setup Time and Minimum Hold time (t_s, t_h, V_{CC} = 1.8 V)

Circuit simulation result



Evaluation circuit

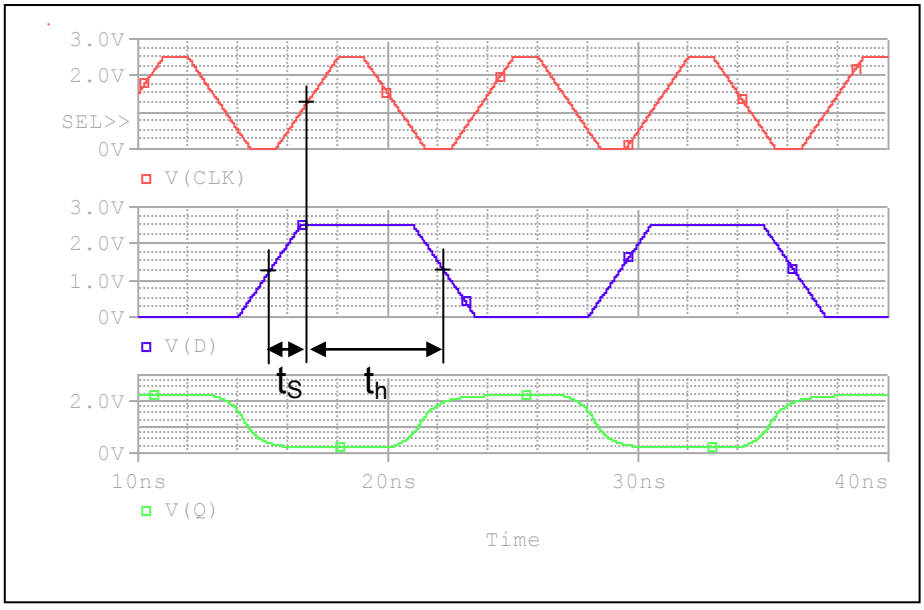


Comparison table C_L = 30 pF, R_L = 500 Ω

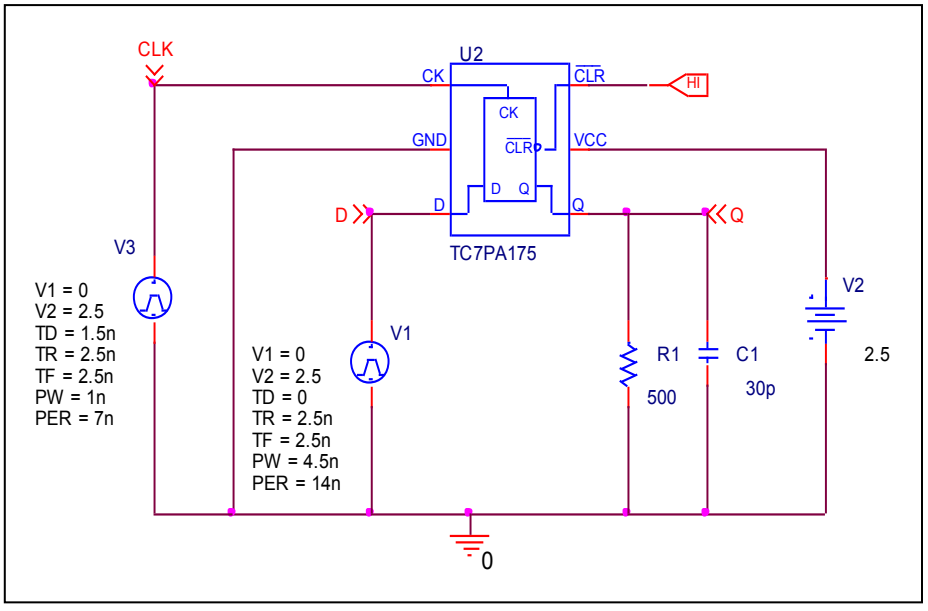
$t_r = t_f$ =3 ns	Measurement	Simulation	Output
t_S (ns)	Min 3.0	3.0	**Active**
t_h (ns)	Min 3.0	13	**Active**

Minimum Setup Time and Minimum Hold time (t_s, t_h, V_{CC} = 2.5 V)

Circuit simulation result



Evaluation circuit

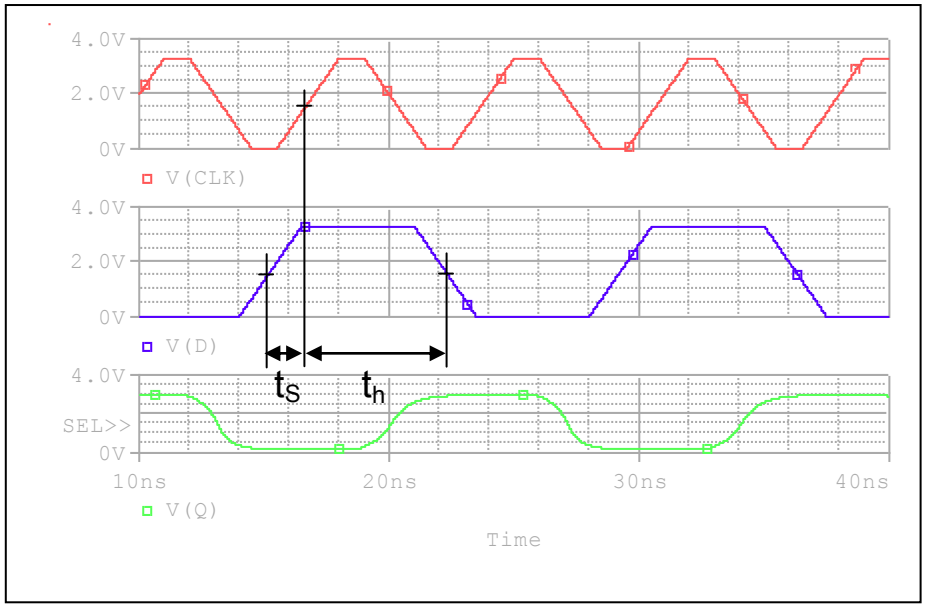


Comparison table C_L = 30 pF, R_L = 500 Ω

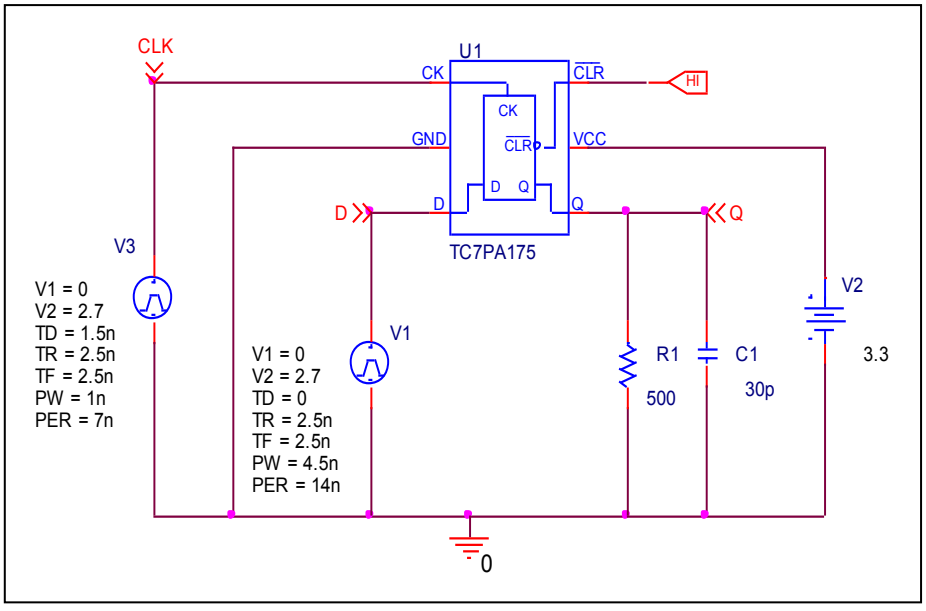
$t_r = t_f$ =3 ns	Measurement	Simulation	Output
t_S (ns)	Min 1.5	1.5	**Active**
t_h (ns)	Min 1.7	5.5	**Active**

Minimum Setup Time and Minimum Hold time (t_s, t_h, V_{CC} = 3.3 V)

Circuit simulation result



Evaluation circuit

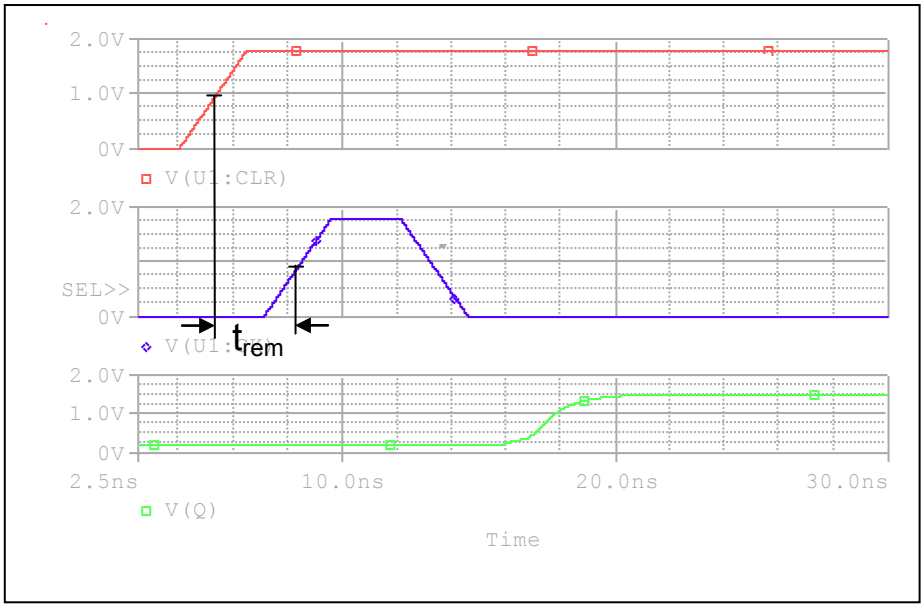


Comparison table C_L = 30 pF, R_L = 500 Ω

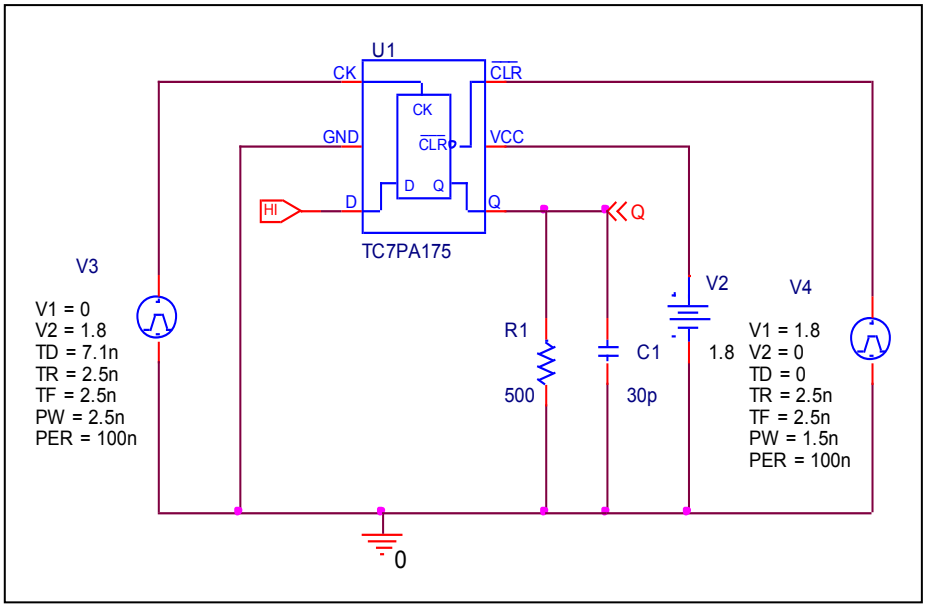
$t_r = t_f$ = 2 ns	Measurement	Simulation	Output
t_S (ns)	Min 1.5	1.5	**Active**
t_h (ns)	Min 1.7	5.5	**Active**

Minimum Removal time (t_{rem}, V_{CC} = 1.8 V)

Circuit simulation result



Evaluation circuit

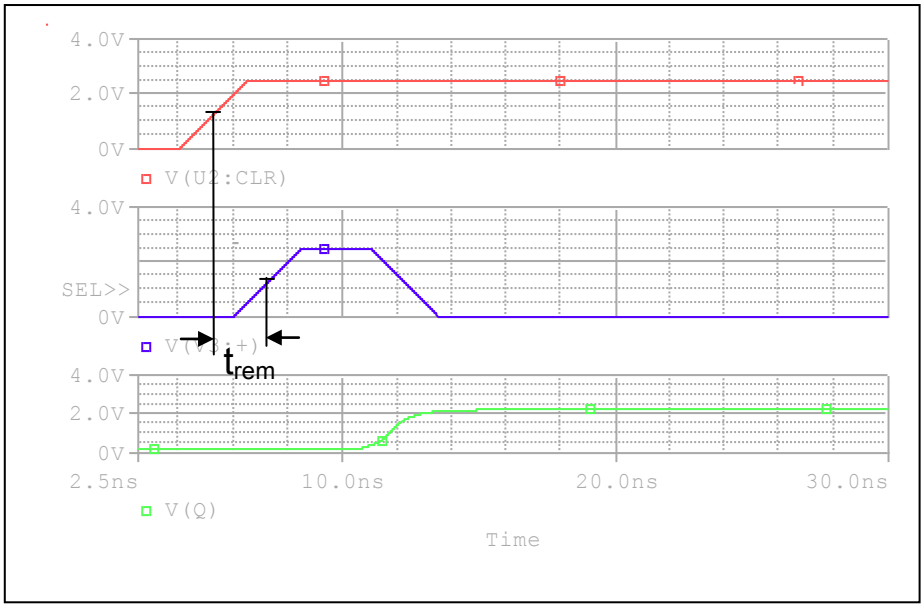


Comparison table **C_L = 30 pF, R_L = 500 Ω**

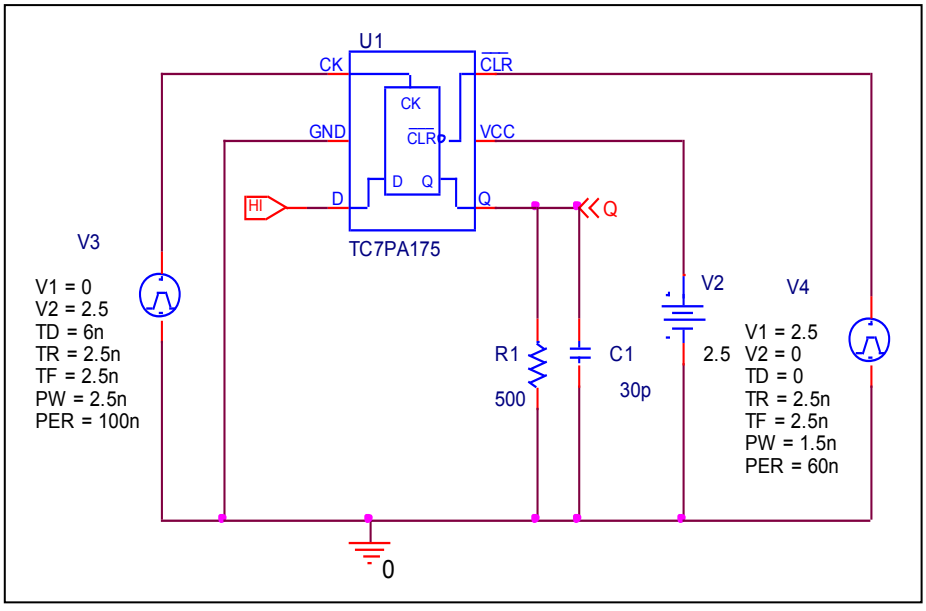
$t_r = t_f$ =3 ns	Measurement	Simulation	Output
t_{rem} (ns)	Min 3.1	3.1	**Active**

Minimum Removal time (t_{rem}, V_{CC} = 2.5 V)

Circuit simulation result



Evaluation circuit

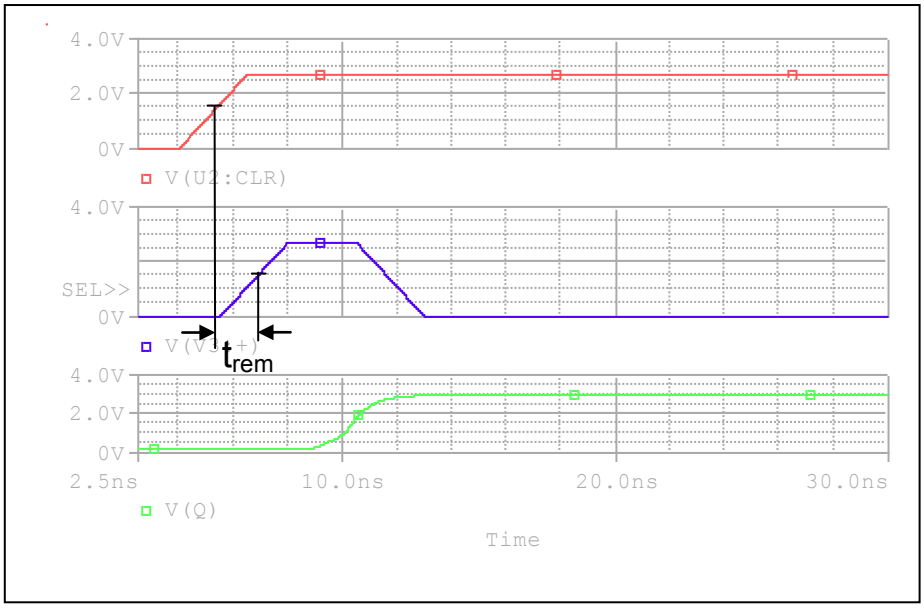


Comparison table **C_L = 30 pF, R_L = 500 Ω**

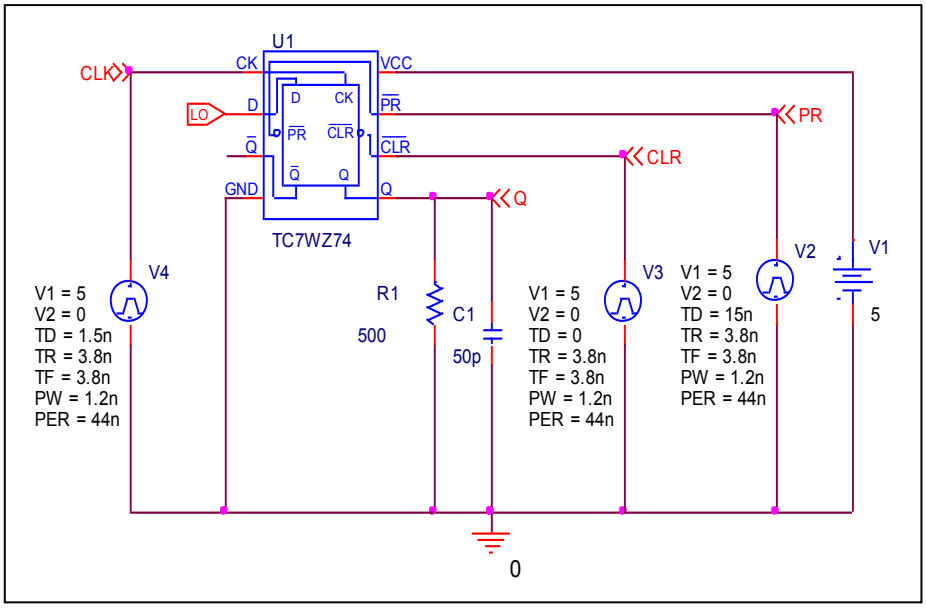
$t_r = t_f$ =3 ns	Measurement	Simulation	Output
t_{rem} (ns)	Min 2.0	2	**Active**

Minimum Removal time (t_{rem}, V_{CC} = 3.3 V)

Circuit simulation result



Evaluation circuit



Comparison table C_L = 30 pF, R_L = 500 Ω

$t_r = t_f$ =3 ns	Measurement	Simulation	Output
t_{rem} (ns)	Min 1.5	1.5	**Active**