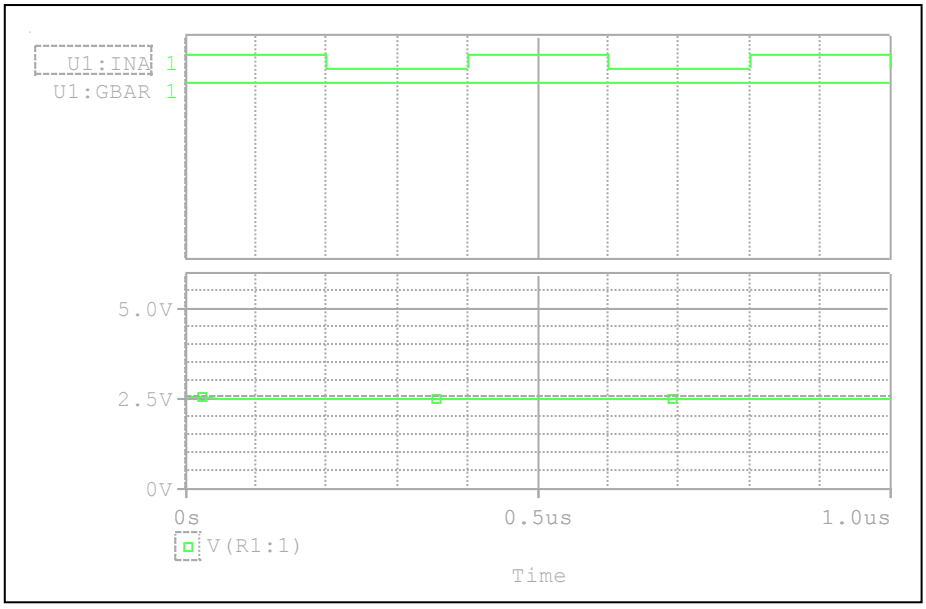
Device Modeling Report

COMPONENTS : CMOS DIGITAL INTEGRATED CIRCUIT
PART NUMBER : TC7SZ125FU
MANUFACTURER : TOSHIBA

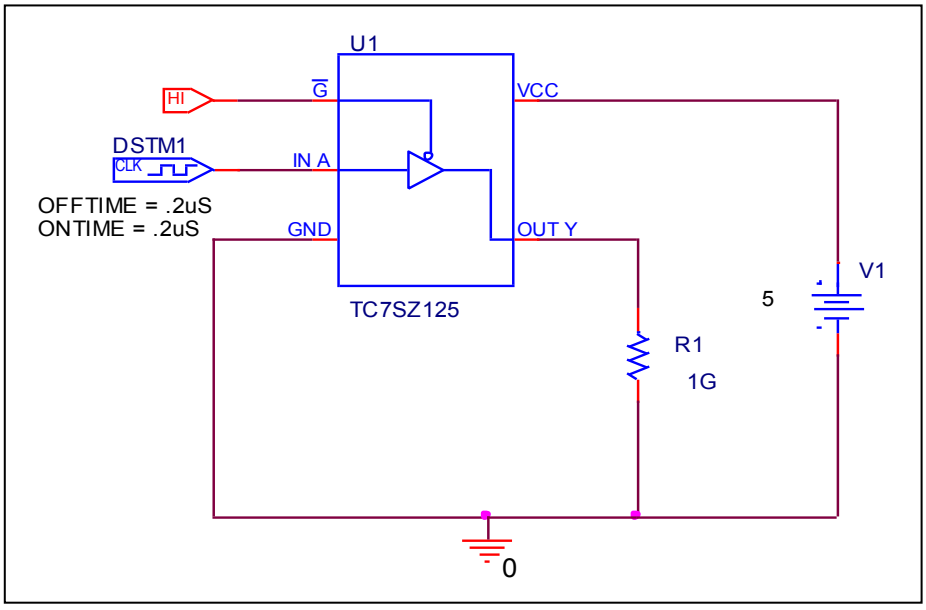
Bee Technologies Inc.

Truth Table

Circuit simulation result



Evaluation circuit

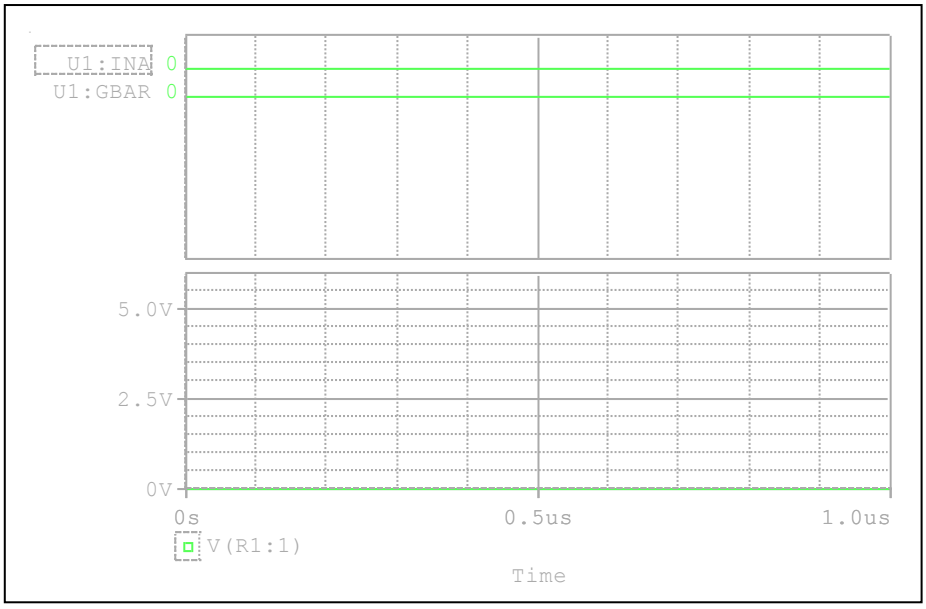


Comparison table

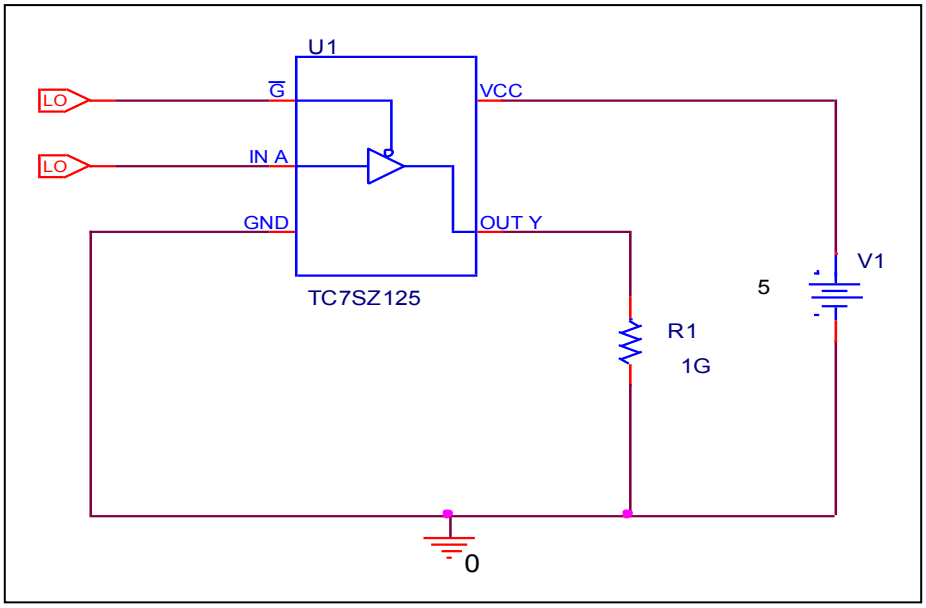
Input		Output		%Error
A	**$\overline{G}$**	**Y (Measurement)**	**Y (Simulation)**	
X	**H**	Z	Z	0

Truth Table

Circuit simulation result



Evaluation circuit

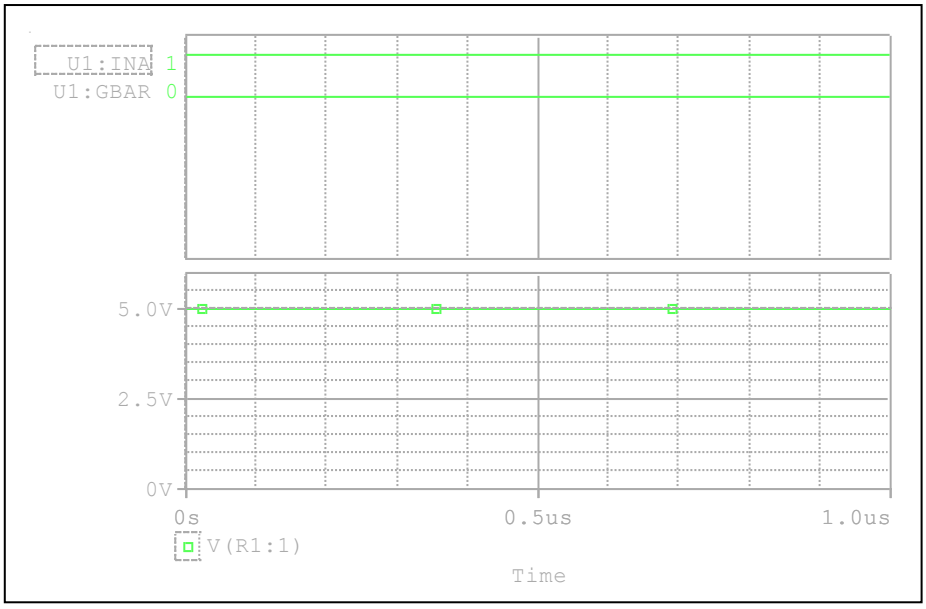


Comparison table

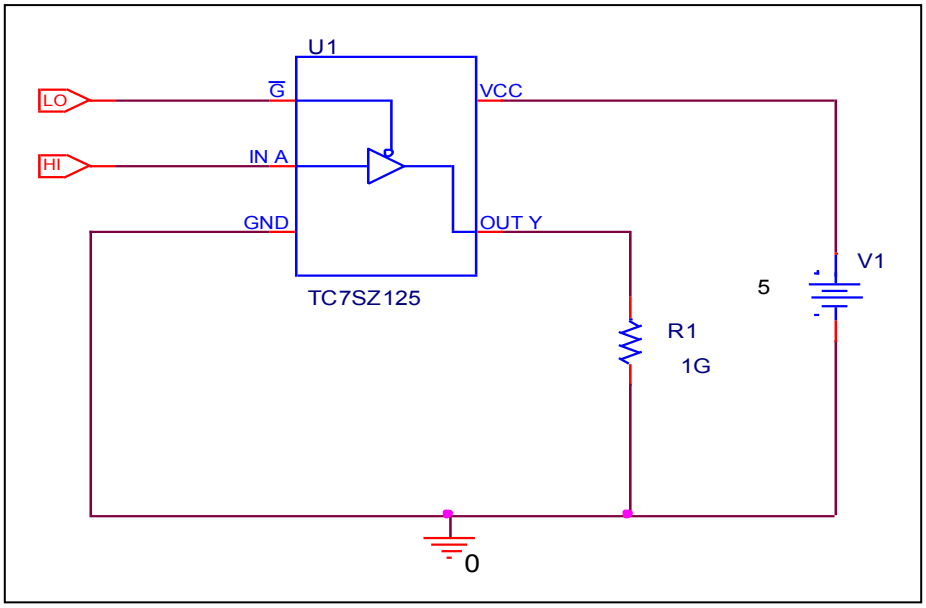
Input		Output		%Error
A	**$\overline{G}$**	**Y (Measurement)**	**Y (Simulation)**	
L	**L**	L	L	0

Truth Table

Circuit simulation result



Evaluation circuit

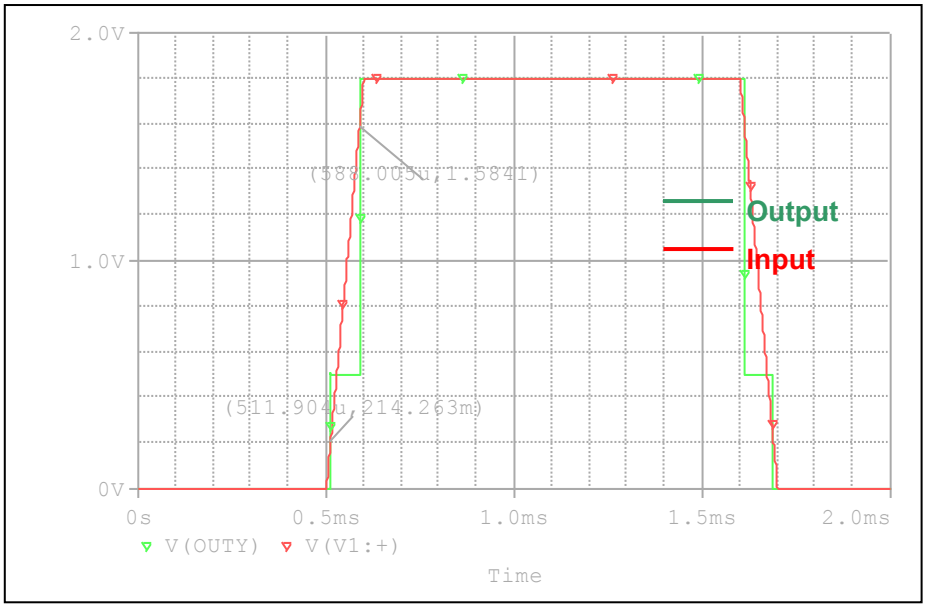


Comparison table

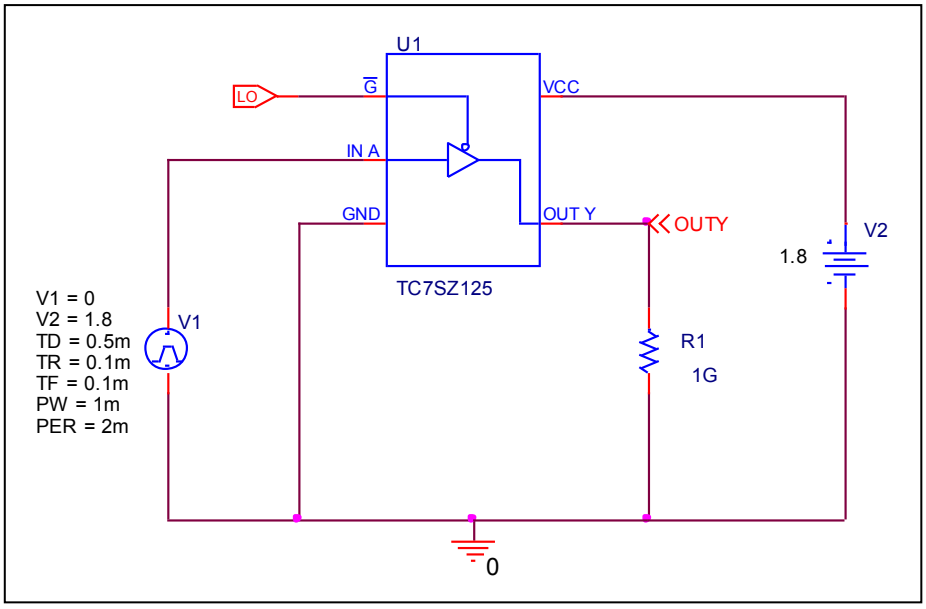
Input		Output		%Error
A	**$\overline{G}$**	**Y (Measurement)**	**Y (Simulation)**	
H	**L**	H	H	0

High Level and Low Level Input Voltage (V_{CC} = 1.8 V)

Circuit simulation result



Evaluation circuit

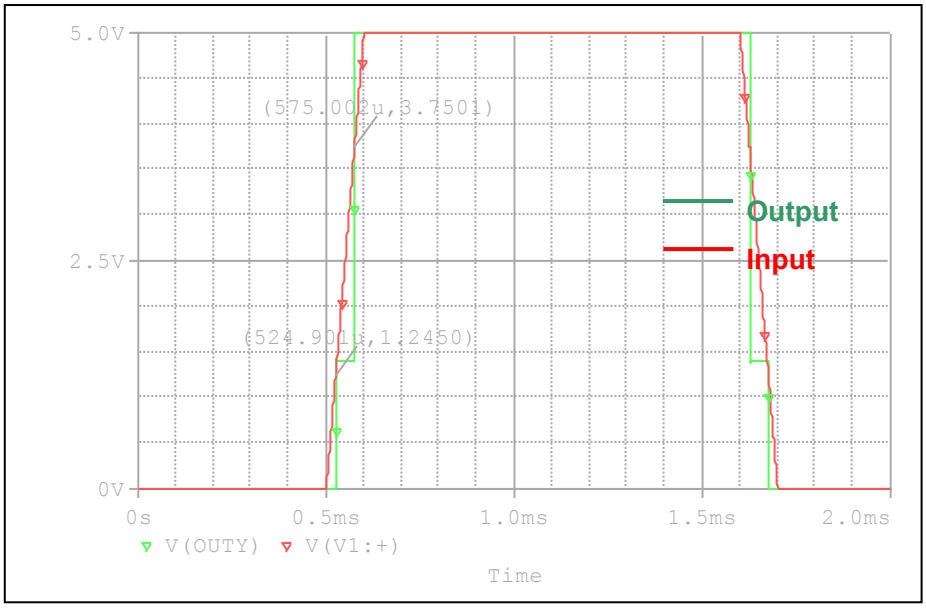


Comparison table

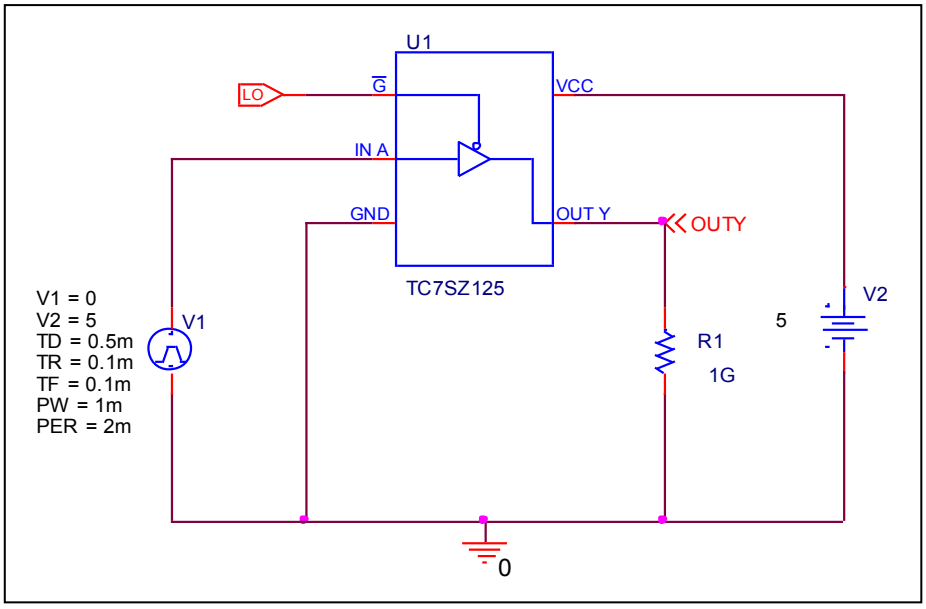
V_{CC} = 1.8V	Measurement	Simulation	%Error
Min V_{IH} = (0.88*V_{CC}) V	1.584	1.5841	0.006
Max V_{IL} = (0.12*V_{CC}) V	0.216	0.214263	-0.804

High Level and Low Level Input Voltage (V_{CC} = 5 V)

Circuit simulation result



Evaluation circuit

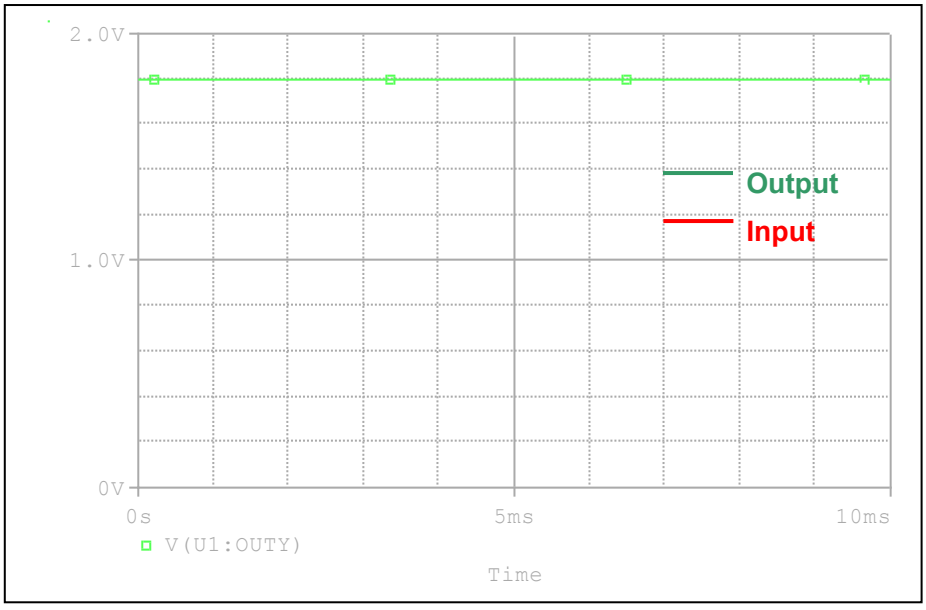


Comparison table

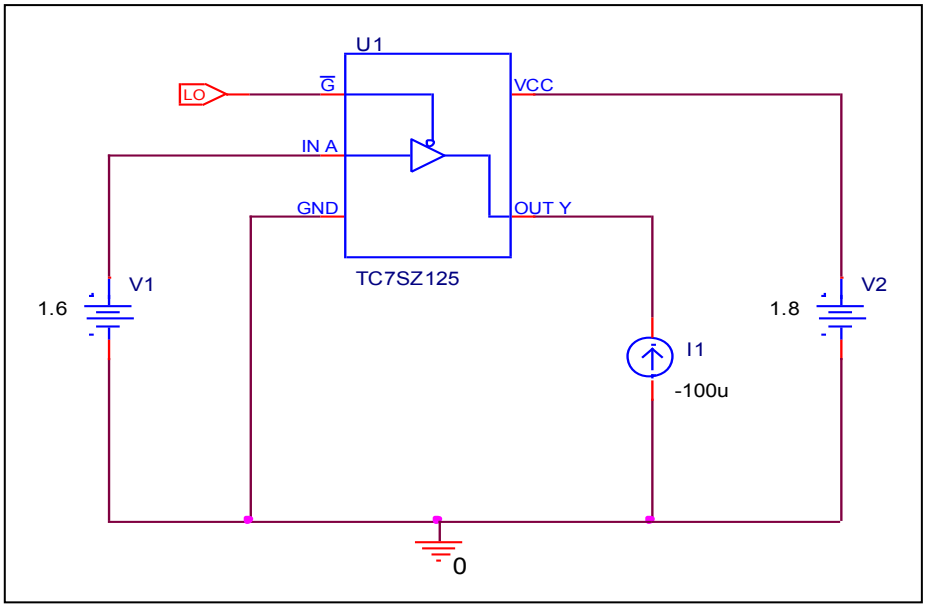
V_{CC} = 5V	Measurement	Simulation	%Error
Min V_{IH} = (0.75*V_{CC}) V	3.75	3.7501	0.003
Max V_{IL} = (0.25*V_{CC}) V	1.25	1.2450	-0.400

High Level Output Voltage (V_{CC} = 1.8 V)

Circuit simulation result



Evaluation circuit

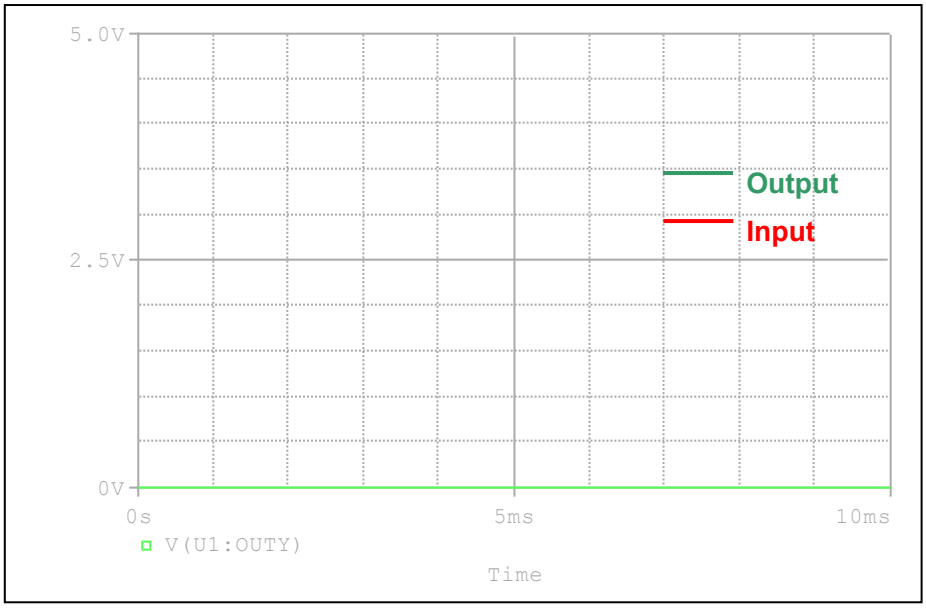


Comparison table

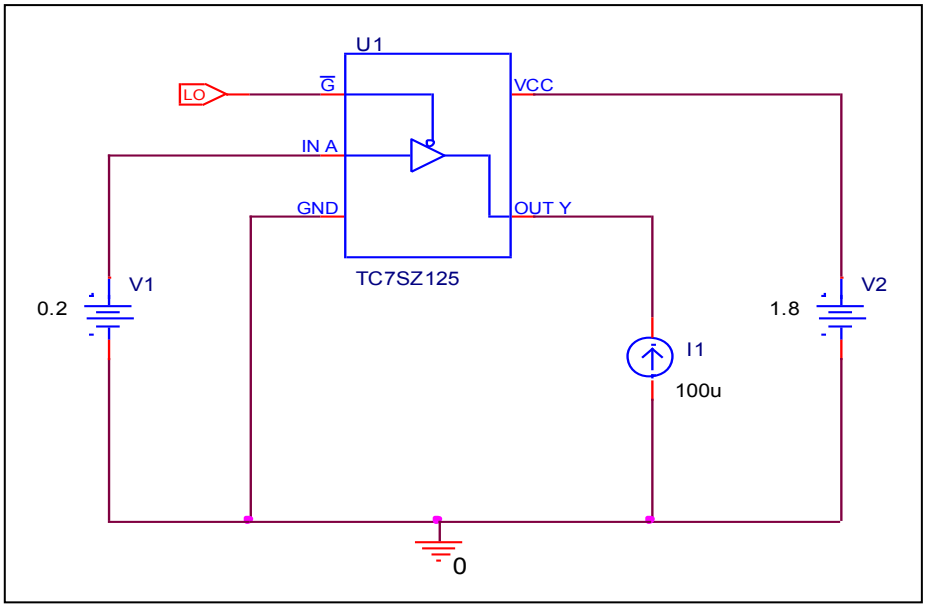
V_{IN} = V_{IH}, V_{CC} = 1.8 V	Measurement	Simulation	%Error
V_{OH} (V)	1.8	1.7999	-0.006

Low Level Output Voltage (V_{CC} = 1.8 V)

Circuit simulation result



Evaluation circuit

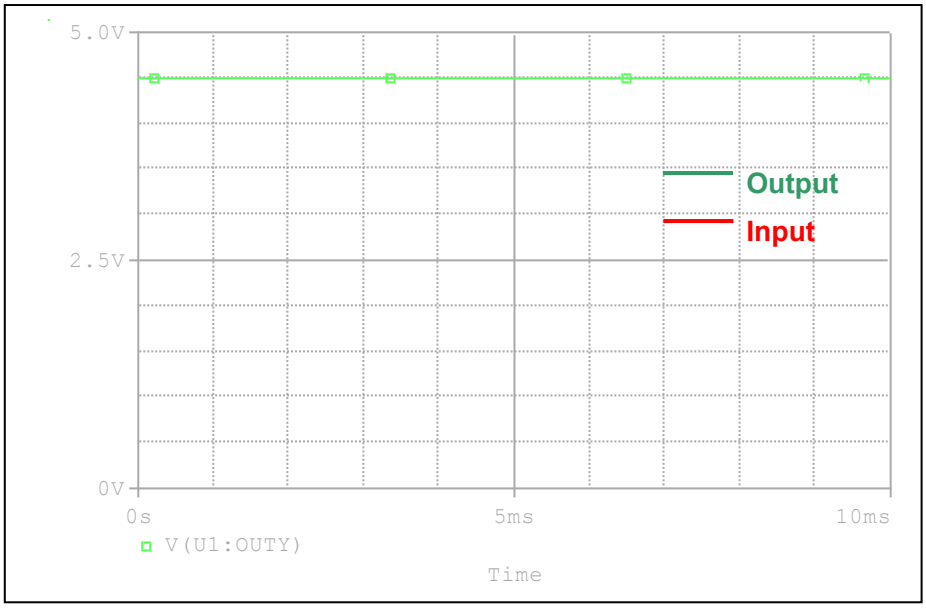


Comparison table

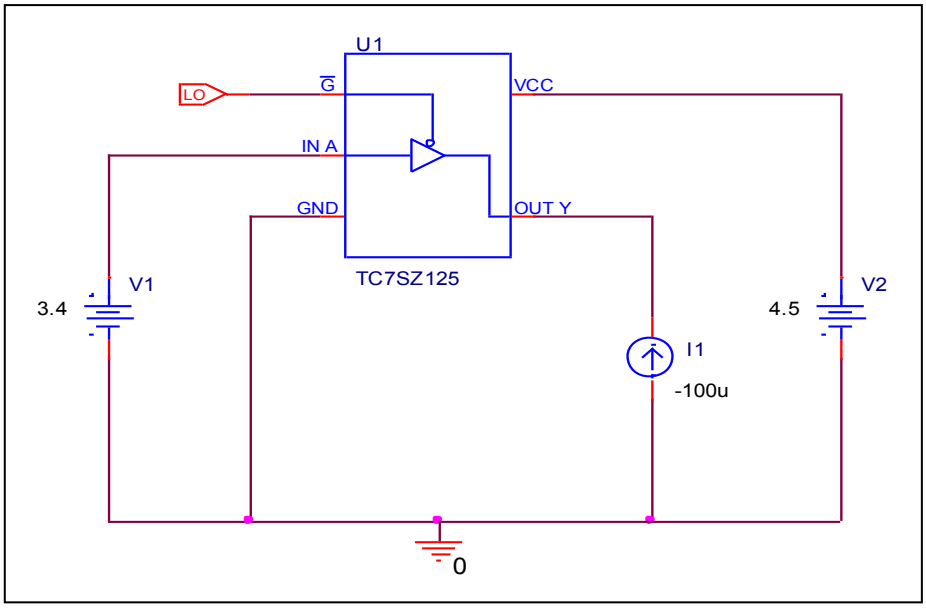
V_{IN} = V_{IL}, V_{CC} = 4.5 V	Measurement	Simulation	%Error
V_{OL} (V)	0	0	0

High Level Output Voltage (V_{CC} = 4.5 V)

Circuit simulation result



Evaluation circuit

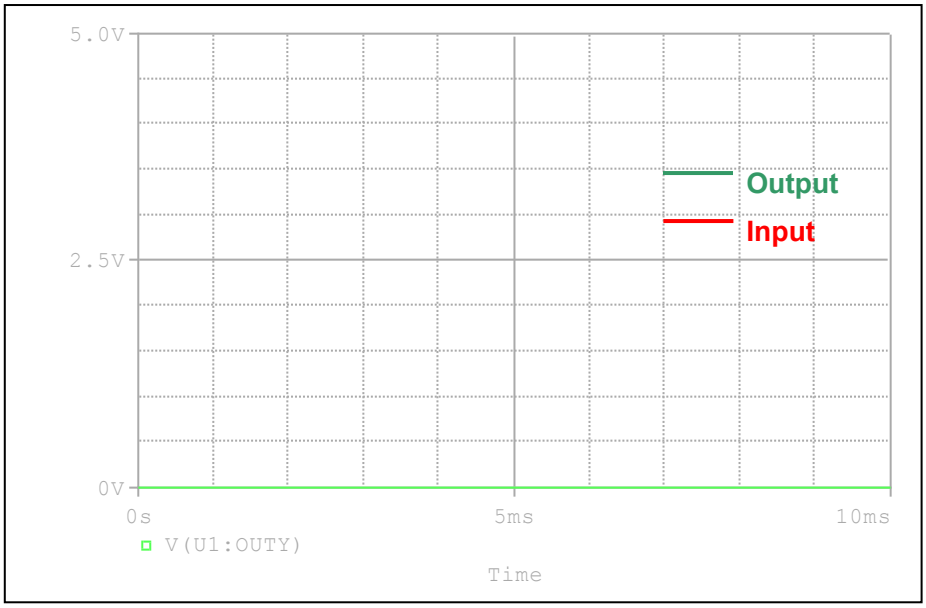


Comparison table

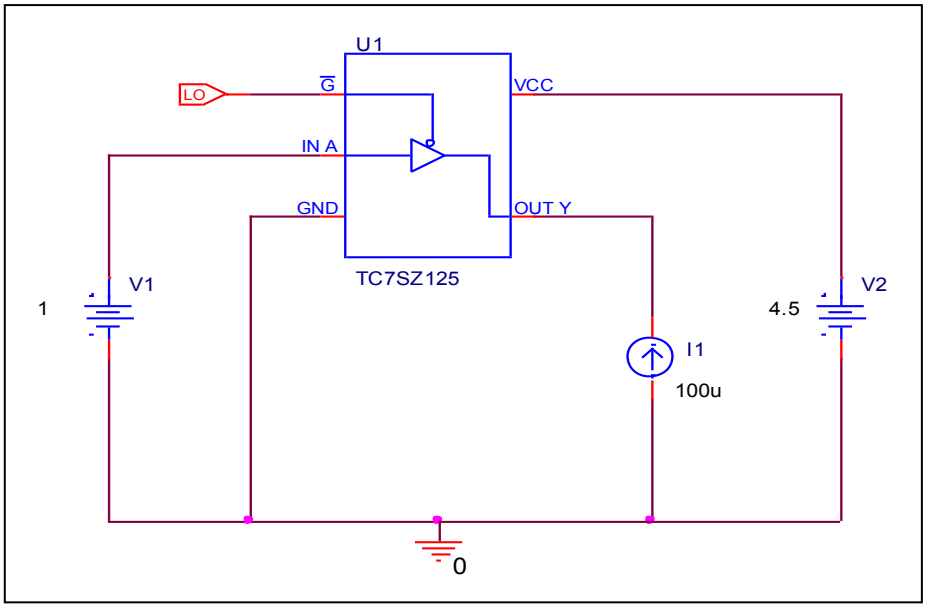
V_{IN} = V_{IH}, V_{CC} = 4.5 V	Measurement	Simulation	%Error
V_{OH} (V)	4.5	4.4991	-0.02

Low Level Output Voltage (V_{CC} = 4.5 V)

Circuit simulation result



Evaluation circuit

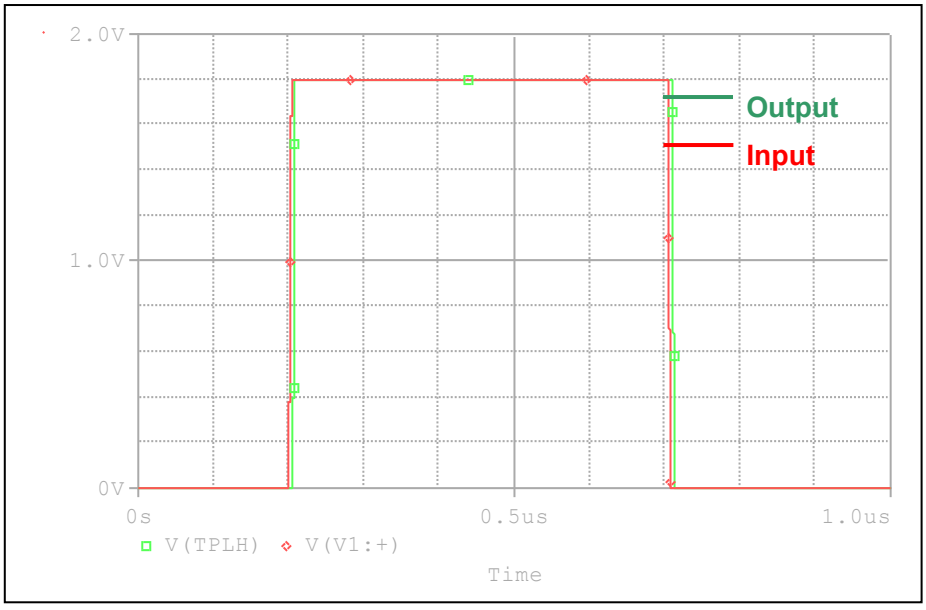


Comparison table

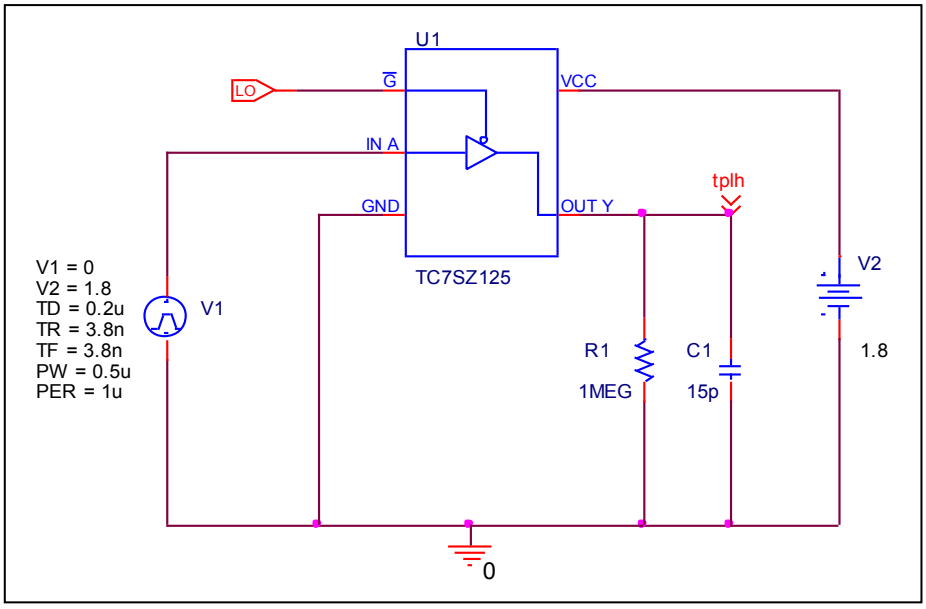
V_{IN} = V_{IL}, V_{CC} = 4.5 V	Measurement	Simulation	%Error
V_{OL} (V)	0	0	0

Propagation Delay Time (V_{CC} = 1.8 V)

Circuit simulation result



Evaluation circuit

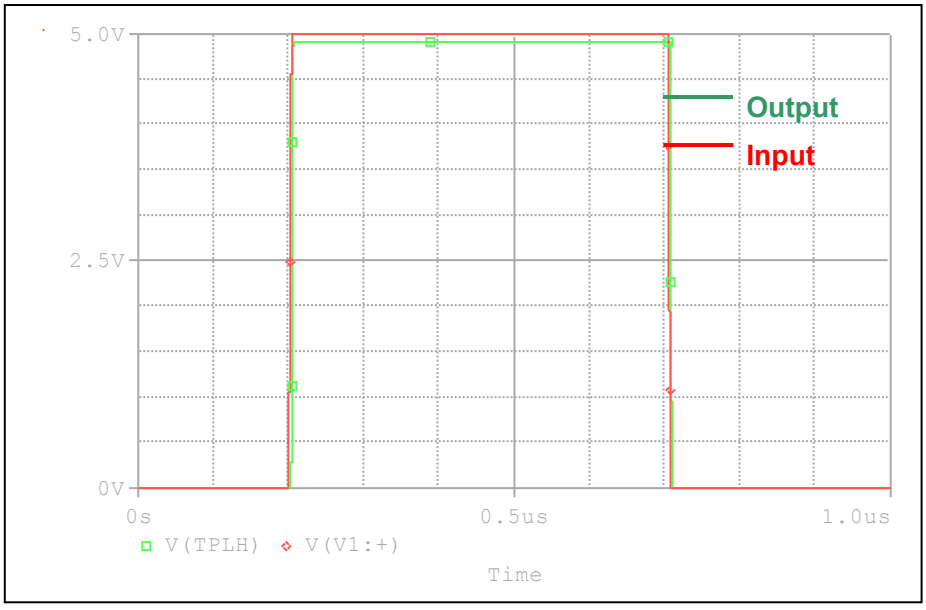


Comparison table C_L = 15 pF, R_L = 1 MΩ

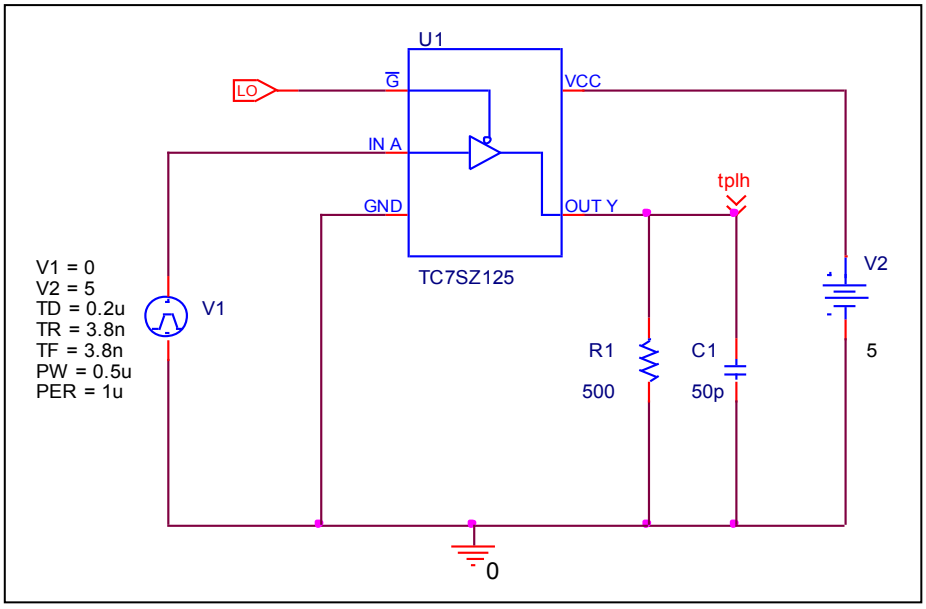
V_{CC} = 1.8V, tr = tf = 3 ns	Measurement	Simulation	%Error
t_{PLH} (ns)	5.3	5.3208	0.392
t_{PHL} (ns)	5.3	5.3079	0.149

Propagation Delay Time (V_{CC} = 5 V)

Circuit simulation result



Evaluation circuit

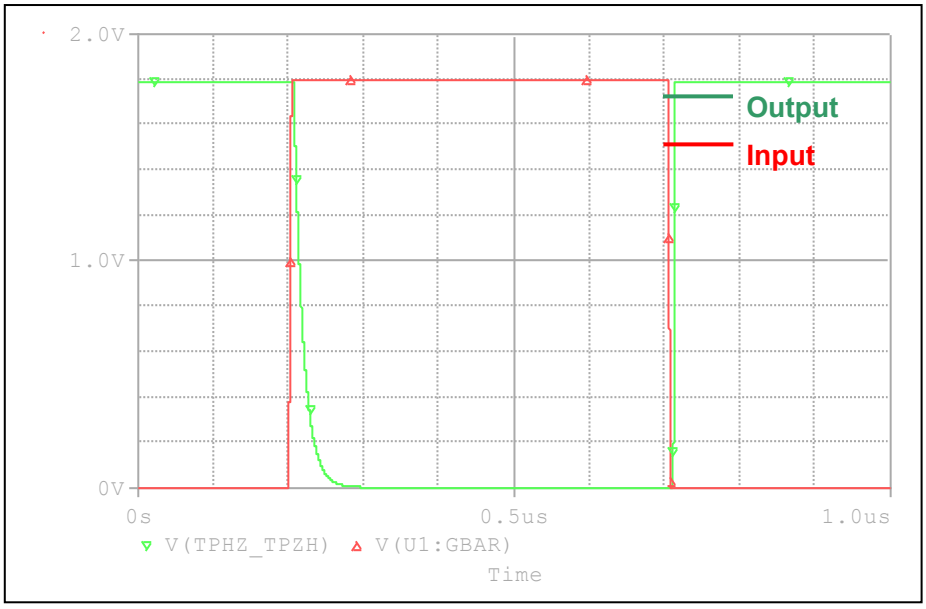


Comparison table C_L = 50 pF, R_L = 500 Ω

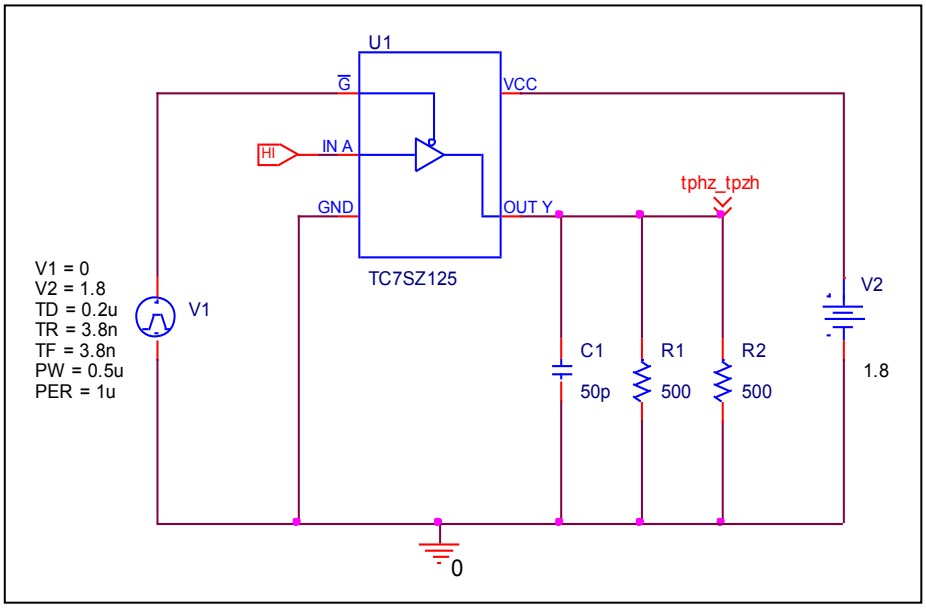
V_{CC} = 5 V, tr = tf = 3 ns	Measurement	Simulation	%Error
t_{PLH} (ns)	2.6	2.6444	1.708
t_{PHL} (ns)	2.6	2.6279	1.073

Output enable time(t_{PZH}) and Output disable time(t_{PHZ}) (V_{CC} = 1.8 V)

Circuit simulation result



Evaluation circuit

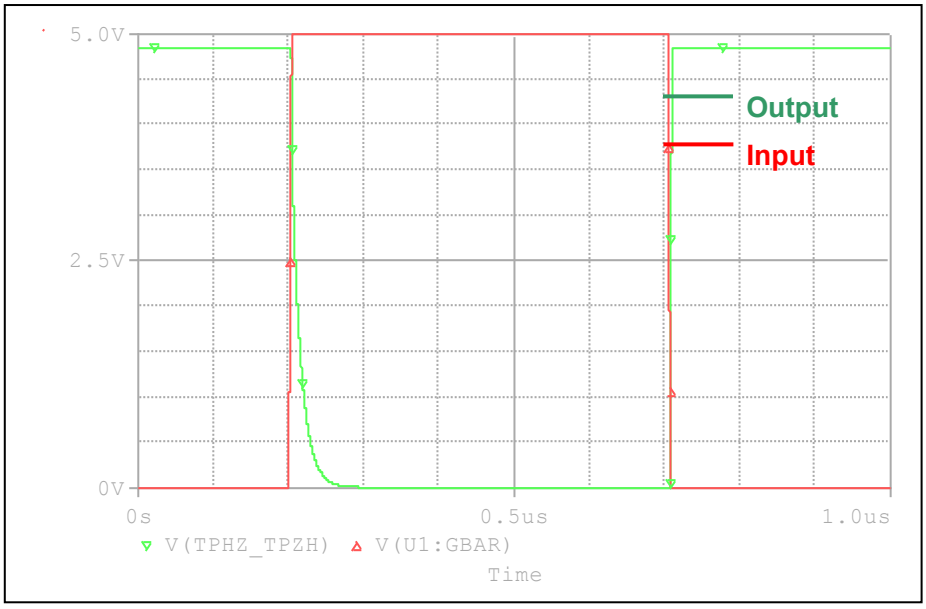


Comparison table C_L = 50 pF, R_L = 500 Ω

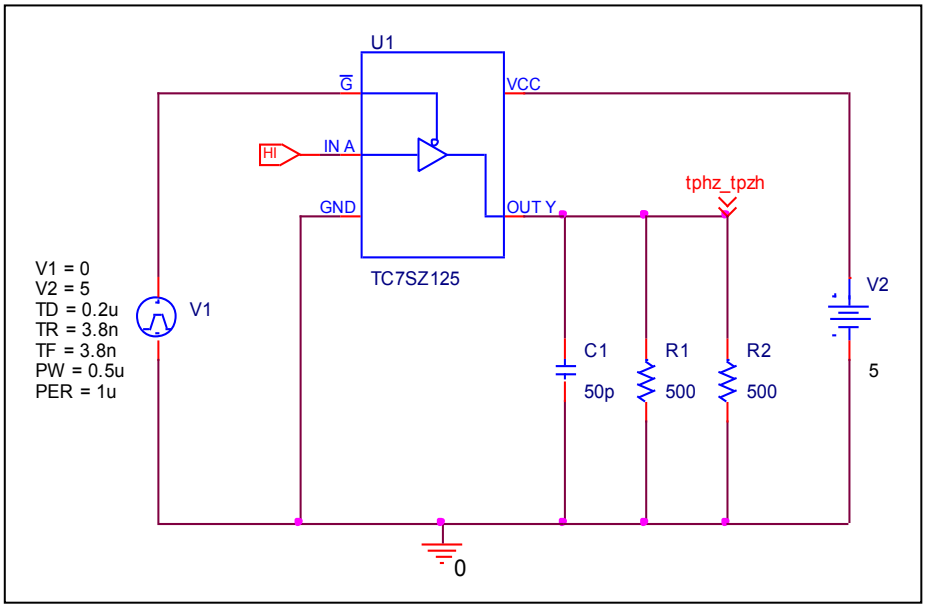
V_{CC} = 1.8V, tr = tf = 3 ns	Measurement	Simulation	%Error
t_{PZH} (ns)	7	7.0535	0.764
t_{PHZ} (ns)	5.4	5.4334	0.619

Output enable time(t_{PZH}) and Output disable time(t_{PHZ}) (V_{CC} = 5 V)

Circuit simulation result



Evaluation circuit

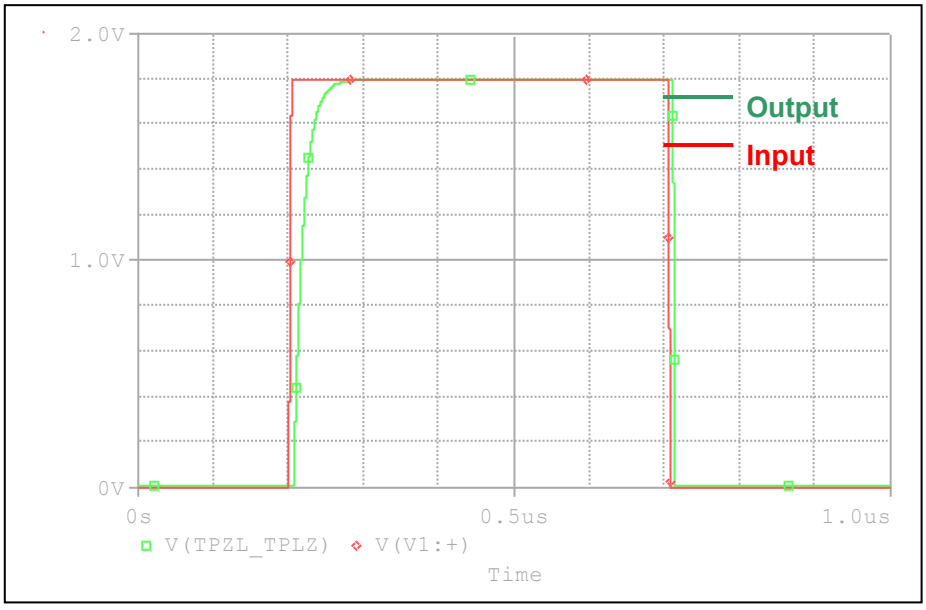


Comparison table C_L = 50 pF, R_L = 500 Ω

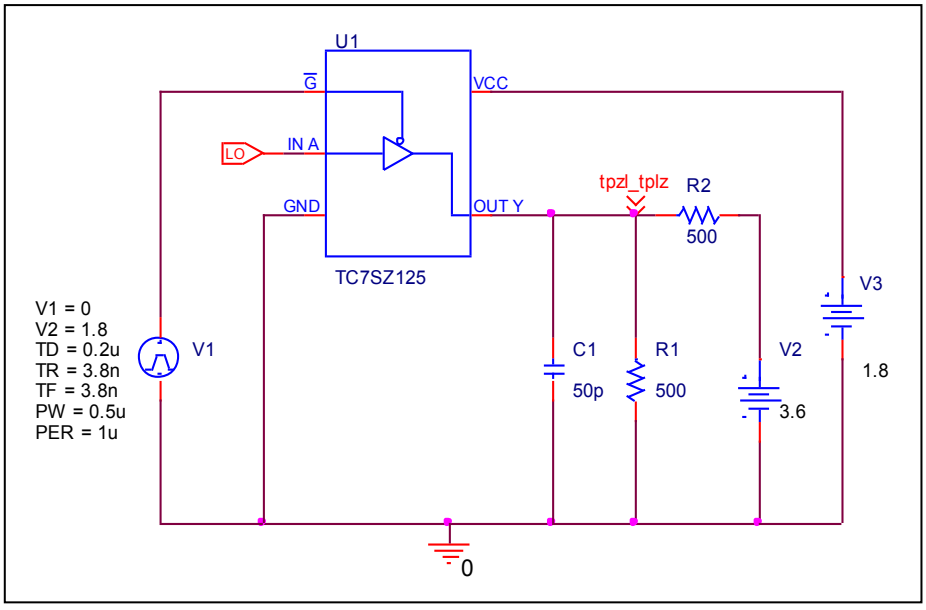
V_{CC} = 5 V, tr = tf = 3 ns	Measurement	Simulation	%Error
t_{PZH} (ns)	2.8	2.7773	-0.811
t_{PHZ} (ns)	2.1	2.1849	4.043

Output enable time(t_{PZL}) and Output disable time(t_{PLZ}) (V_{CC} = 1.8 V)

Circuit simulation result



Evaluation circuit

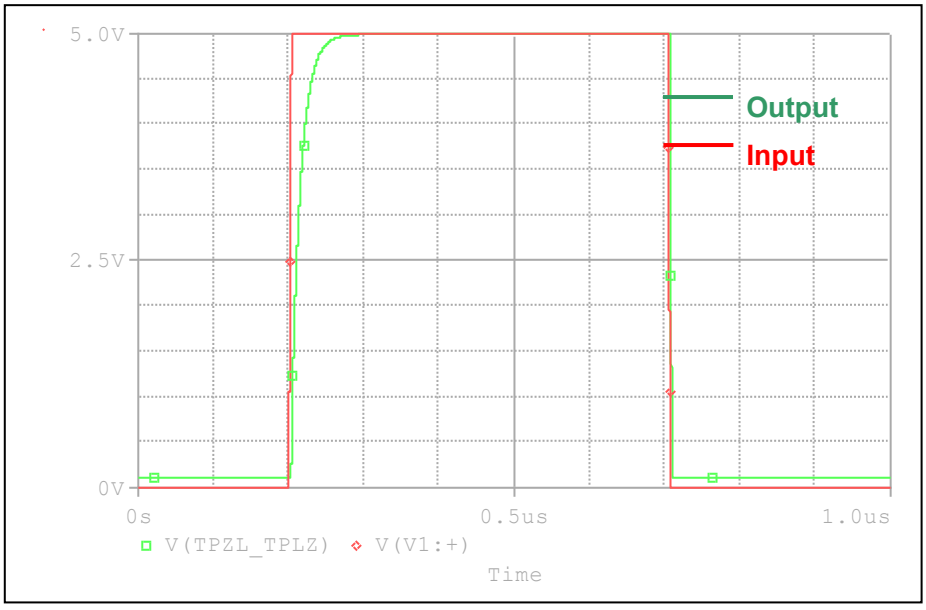


Comparison table C_L = 50 pF, R_L = 500 Ω

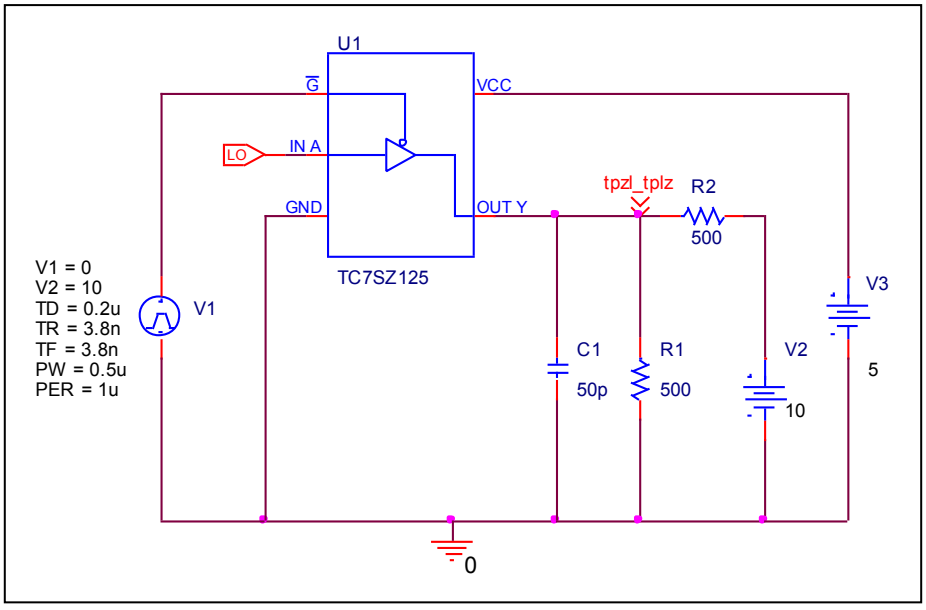
V_{CC} = 1.8 V, tr = tf = 3 ns	Measurement	Simulation	%Error
t_{PZL} (ns)	7	7.0213	0.304
t_{PLZ} (ns)	5.4	5.4336	0.622

Output enable time(t_{PZL}) and Output disable time(t_{PLZ}) (V_{CC} = 5 V)

Circuit simulation result



Evaluation circuit



Comparison table C_L = 50 pF, R_L = 500 Ω

V_{CC} = 5 V, tr = tf = 3 ns	Measurement	Simulation	%Error
t_{PZL} (ns)	2.8	2.7927	-0.261
t_{PLZ} (ns)	2.1	2.1048	0.229